

Making Open Silicon Design Everywhere

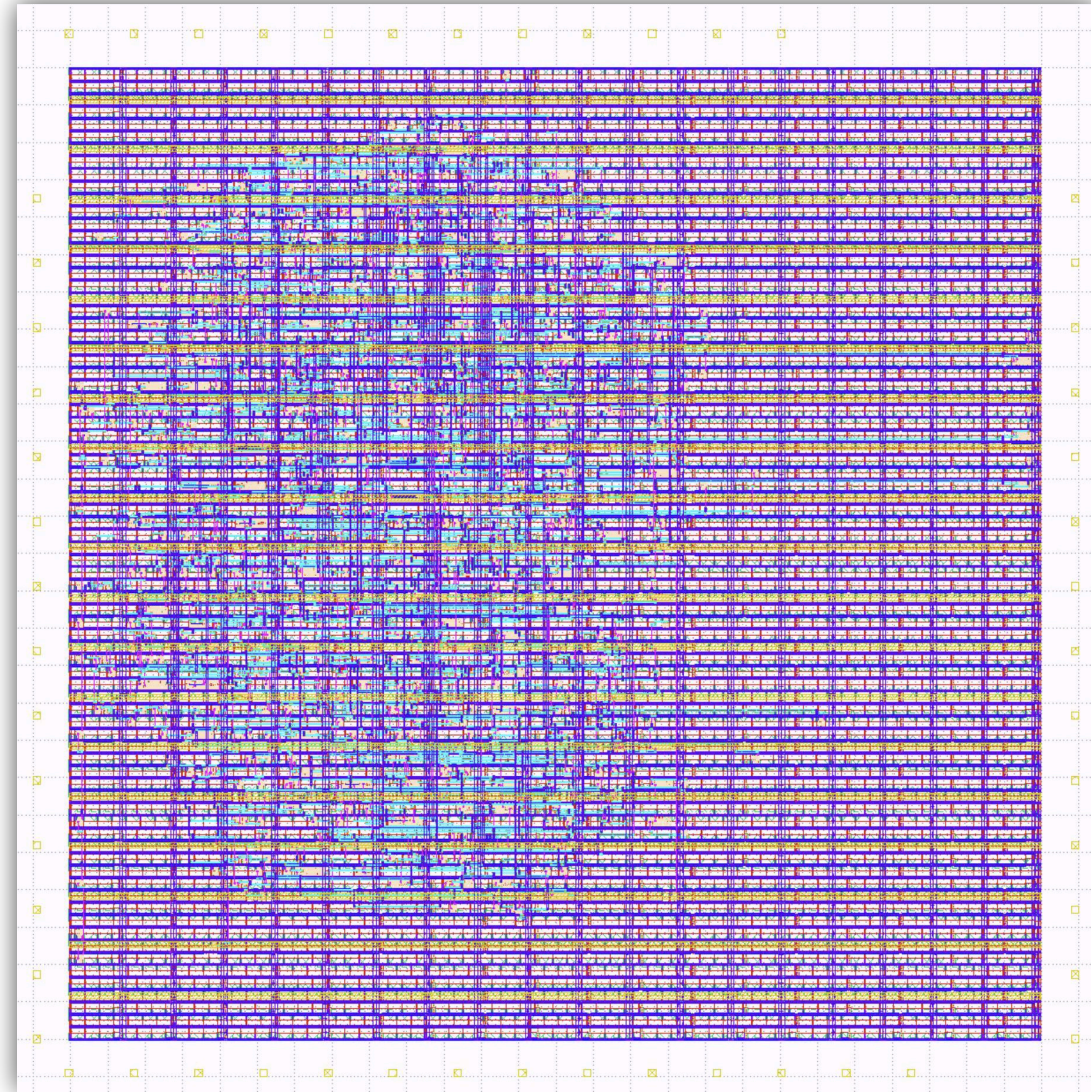
Using Cloud-based Open Agile EDA Platform

Xueyan Zhao*, Hao Wang, Yuchi Miao, Zhipeng Huang, Zhisheng Zeng,
Zengrong Huang, Simin Tao, Yujia Peng, Chunan Zhuang, Xiaoke Su, Yuyang
Miao, Guiyu Dai, Hao Li, **Tong Liu, Zihao Yu, Xingquan Li, Biwei Xie, Yungang
Bao**

ECOS Team of Center for Advanced Computer Systems,
Institute of Computing Technology, Chinese Academy of Sciences
Free Silicon Conference 2025 – IHP, Frankfurt (Oder), Germany
July 2-4, 2025

FSiC2025
Free Silicon Conference

Xueyan Zhao, Hao Wang and Yuchi Miao are co-authors, * means **speakers**

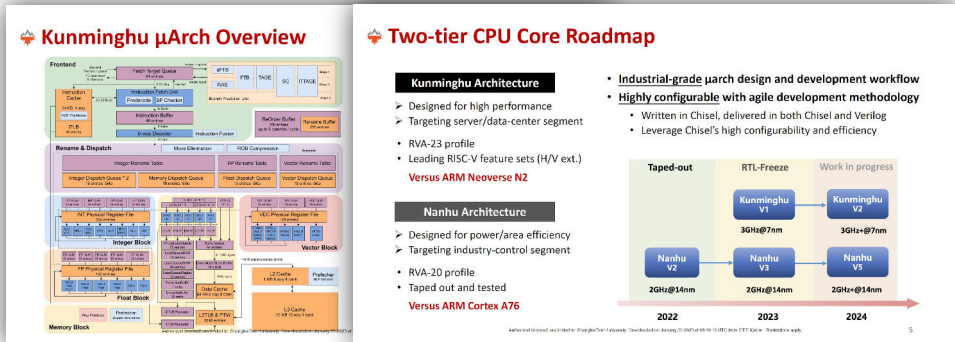


About us (Build Open Silicon Ecosystem!)

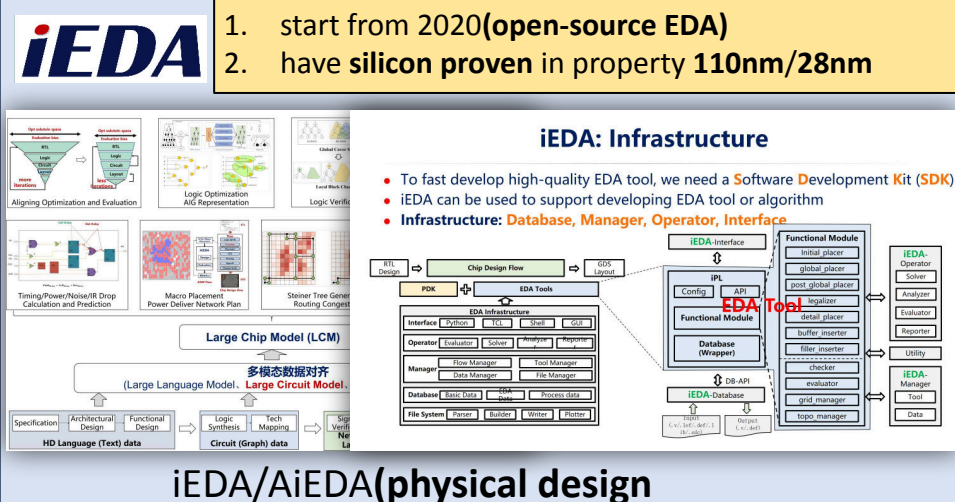
- A real BIG team from China (ICT, BOSC and PCL, >100 persons, led by Prof. Yungang Bao)



1. start from 2020(>6K stars, >730 fork on Github)
2. highest performing open-source processor series



Xiangshan(processor)



2020 tools)

ECOS TEAM

we ARE
HERE(*^▽^*)

clusterIP
(IP components)

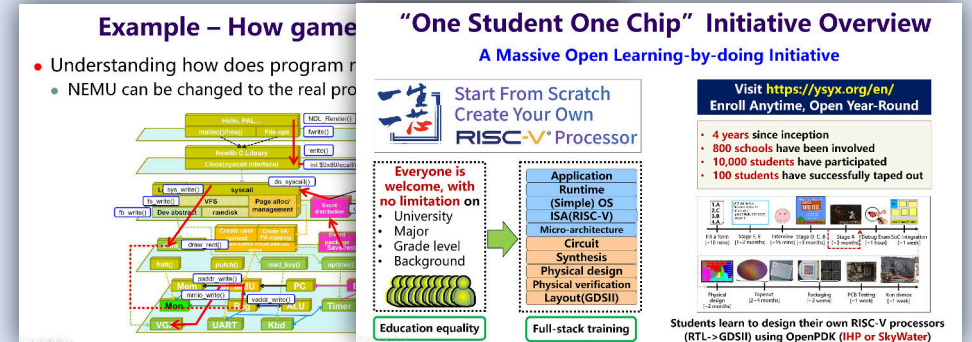
ChipCompiler
(design flow)

ECOS Studio
(cloud platform)

FSiC 2025



1. start from 2019(involve 12000+ students in China)
2. provide FREE frontend and backend courses online



"One Student One Chip" Initiative(education)

SNOW

1. start from 2024(focus on open ASIC design service)
2. integrate IP components, flow and cloud platform



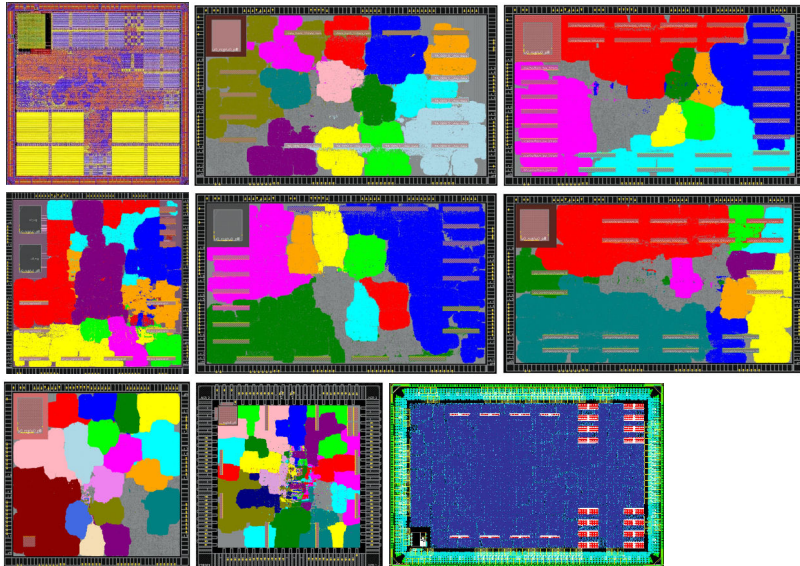
SNOW(Shuttle-NO-Wait, design service)

2/27

ECOS Team: Provide ASIC Full-stack Solutions

- tape-out **10+** chips/year (**IP Design/SoC Integrate/Physical Design/Package/Bring-up**)
 - cover **130/110/55/40/28nm**, **10K~10M** instances, **100MHz ~ 1.5GHz**, multiple power/clock domains
 - design open-source processors (**can boot Linux**) and Ips (UART, TIMER, QSPI, I2S, I2C, VGA, PSRAM...)
 - develop **iEDA** (iEDA just **focus on PD stage now**)
 - serve students and several institutions (**One Student One Chip, NU. Kazakhstan, ...**)
 - develop ECOS Studio (**cloud platform**) with **Yosys+iEDA** based on **ICS55 Open PDK** (ongoing)

Some tape-outed chips of our team:



"One Student One Chip" Initiative

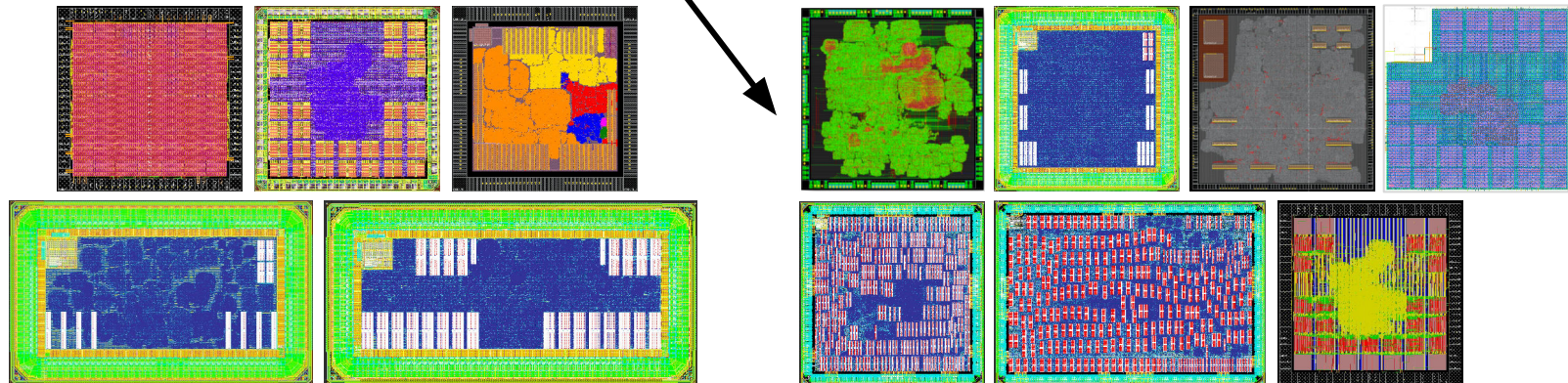
2025/7/4

The Open Silicon Technical Roadmap of ECOS Team

2021-2024: Property EDA (**synthesis, floorplan**) and iEDA (**PD stage**) mixed use

2022-2025: **Develop** and try open-source flow based on **iEDA** and **SKY/IHP130/ICS55 PDK**

2025-2030: **Open** FULL RTL2GDS flows (**Yosys+iEDA+ICS55 Open PDK on ECOS Studio**)



External Collaboration Project

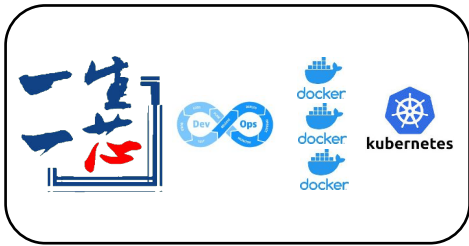
FSiC 2025

Tape-out by using iEDA in 110/55/28nm

3/27

Highlight

- Teach physical design with cloud platform **ECOS Studio (Yosys + iEDA + ICS55)**
- Introduce an education-oriented chip **retroSoC** tape-outed in **SMIC/SKY130**
- Share some of the latest information on iEDA toolchains



+



+



章节安排

整个讲义按照逻辑，并通过动手本，这一章将得到可流片的 SoC 和 iEDA 后端的物理设计。本章所介绍的高级技术和积累，本章所介绍的流片 SoC 获得更多后端工

从晶体管的视角看后端

在初探芯片后端物理设计这一章中大家已经了解到芯片在微观尺度上主要是由 CMOS 晶体管和互连网络组成的。晶体管在微观尺度上的特性会在很大程度上决定芯片在宏观世界的运行结果。这意味着只有当大家开始尝试站在晶体管的视角去思考问题时，才能抽丝剥茧，发现隐藏在现象背后的本质。而这对于大家掌握物理设计流程的有关概念以及采用的优化手段是十分重要的。举个例子，现在给出一个典型的 CMOS 反相器的逻辑表达式、原理图、物理模型以及电压传输特性 (VTC)：

MODEL → LOGIC → PHYSICS → VTC

理想 CMOS 反相器原理图和传输特性 1

对于一个理想的 CMOS 反相器来说，其中 V_{in} 为信号输入， V_{out} 为信号输出， V_{th} 为阈值电压（假定 NMOS 和 PMOS 阈值大小一样），则其功能表达如下：

- 当 $V_{in} < V_{th}$ 时， V_{out} 保持逻辑高电平不变。
- 当 $V_{in} = V_{th}$ 时， V_{out} 从逻辑高电平变成逻辑低电平。
- 当 $V_{in} > V_{th}$ 时， V_{out} 保持逻辑低电平不变。

上图中反相器抽象模型（非门）和逻辑表达式（原理图）是大家在学完数字电路基础后对“非门”的认识。“非门”是一种理想的逻辑表达，由这种理想模型构建起的互联网络也是理想的，这是数字前端设计在建模时首先采用的逻辑模型。但是处于真实芯片世界的 CMOS 反相器和互联模型要远比这个复杂：

- 受限半导体制造工艺精度，CMOS 反相器切换状态存在时延。
- 传输线和负载的电容和电感对 CMOS 反相器的带载能力和传输特性会产生影响。

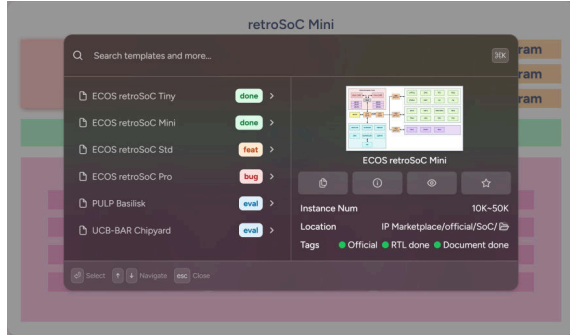
cluster	IP	development state	
system	Common Component, Interrupt Controller, Reset&Clock Unit		
	common	SPC done RTF done SMT done UVV no FUC 0 CDC 0 SOI done FPE done TPT done	
	archinfo	SPC done RTF done SMT done UVV no FUC 0 CDC 0 SOI done FPE done TPT done	
	clint	SPC done RTF done SMT done UVV no FUC 0 CDC 0 SOI done FPE done TPT done	
plic	SPC done RTF done SMT done UVV no FUC 0 CDC 0 SOI done FPE done TPT no		
	rcu	SPC done RTF done SMT done UVV no FUC 0 CDC 0 SOI done FPE done TPT done	
	interface	Low-speed Peripherals	
		gpio	SPC done RTF done SMT done UVV no FUC 0 CDC 0 SOI done FPE done TPT done
uart		SPC done RTF done SMT done UVV no FUC 0 CDC 0 SOI done FPE done TPT done	
ps2		SPC done RTF done SMT done UVV no FUC 0 CDC 0 SOI done FPE done TPT done	
timer	SPC done RTF done SMT done UVV no FUC 0 CDC 0 SOI done FPE done TPT done		
	pwm	SPC done RTF done SMT done UVV no FUC 0 CDC 0 SOI done FPE done TPT done	
	wdg	SPC done RTF done SMT done UVV no FUC 0 CDC 0 SOI done FPE done TPT done	
	rtc	SPC done RTF done SMT done UVV no FUC 0 CDC 0 SOI done FPE done TPT done	
application	Specific Field IPs		
	img	SPC done RTF done SMT done UVV no FUC 0 CDC 0 SOI done FPE done TPT done	

WHY we develop ECOS Studio ?

- Get more students excited about open silicon design (**just for fun!**)
 - encourage enthusiasts share their ideas or thinkings with the community
 - help more students involved in EDA algorithm (**design a simple synthesis tool~**)
- Fill the gap between **industry** and **academic (community-oriented)**
 - property tools are incredibly expensive and **uncontrolled** (geopolitical uncertainties)
 - increasing **actual demands** from industry back to academic
 - new EDA algorithms from academic need a series of trials before applying to industry
- Erase performance differences from local computer (**using cloud clusters!**)
 - physical design tools eat **too much memory** and **CPU resources (T o T)**
 - meet different learners' needs from different **countries** and **regions**
- Provide an **OPEN** solution for the potential commercial marketplace

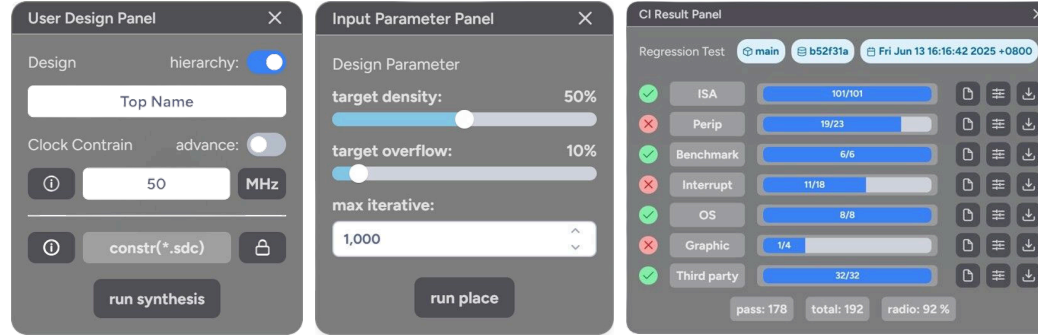
SoC Template

Select SoC template from the IP Market

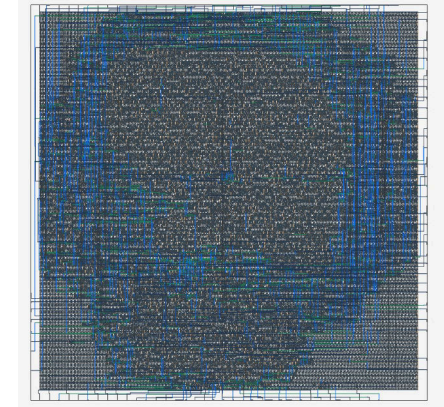


Float Panel System

Support the dragging, resizing operations and customized data



Advanced eXtensible Layout Editor



Cloud-based Agile EDA Platform

iEDA Inside

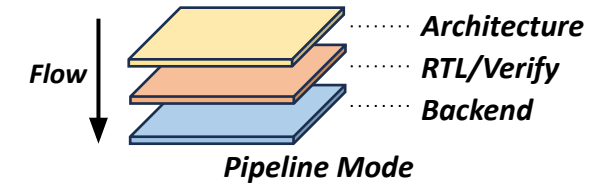
“An open-source EDA infrastructure”
(support ICS55/SKY130/IHP130)



ECOS Studio
“Componentization of Data”

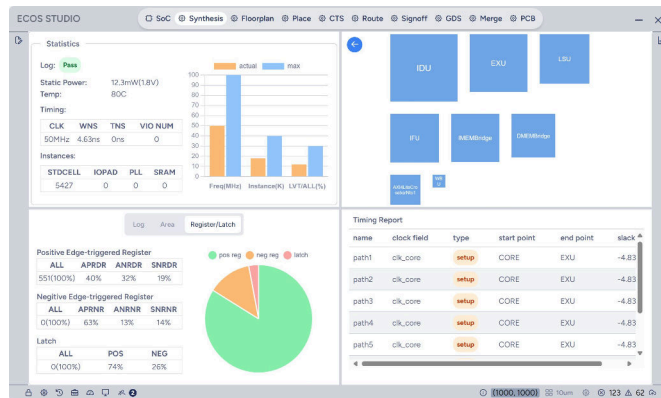


Real-time Collaboration*

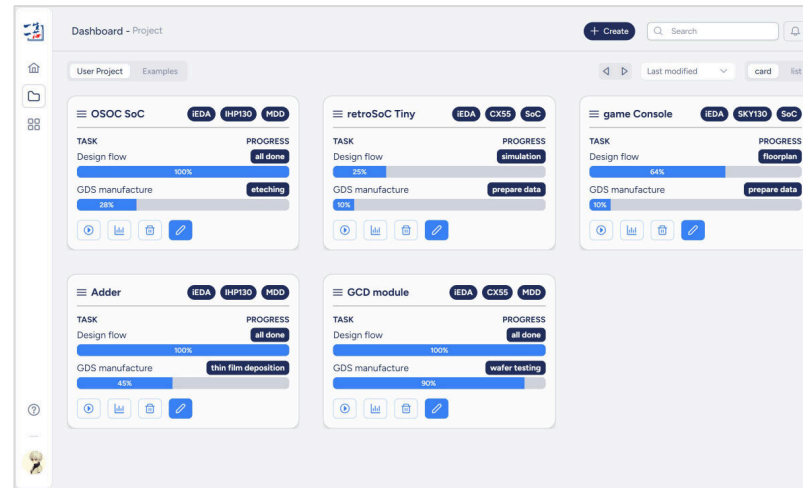


*: this feature will be released in 2025Q4

Synthesis Flow

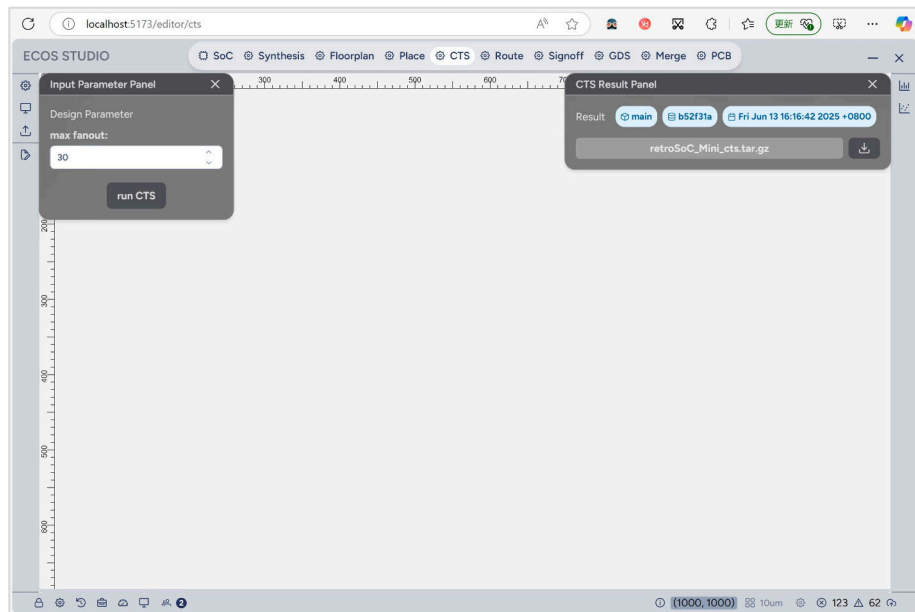
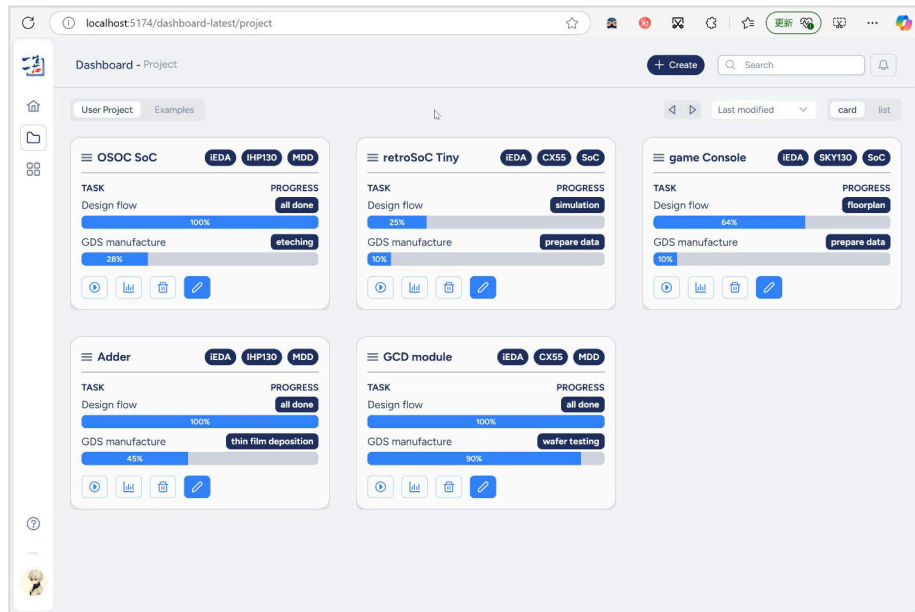


Dashboard



Merge to Latest Shuttle





Partial Key Processes

Create Project

1. fill project name
2. add social info
3. select license

Run Placement

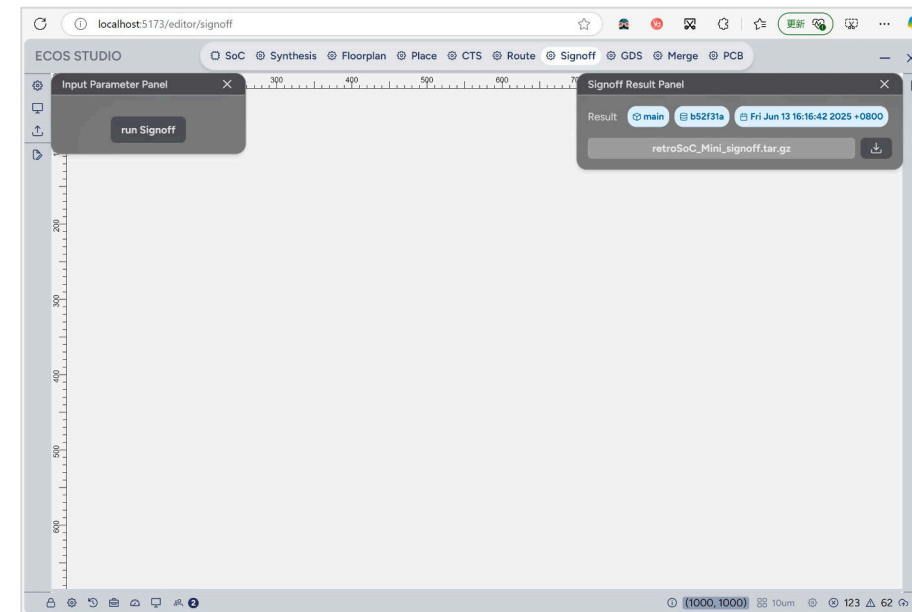
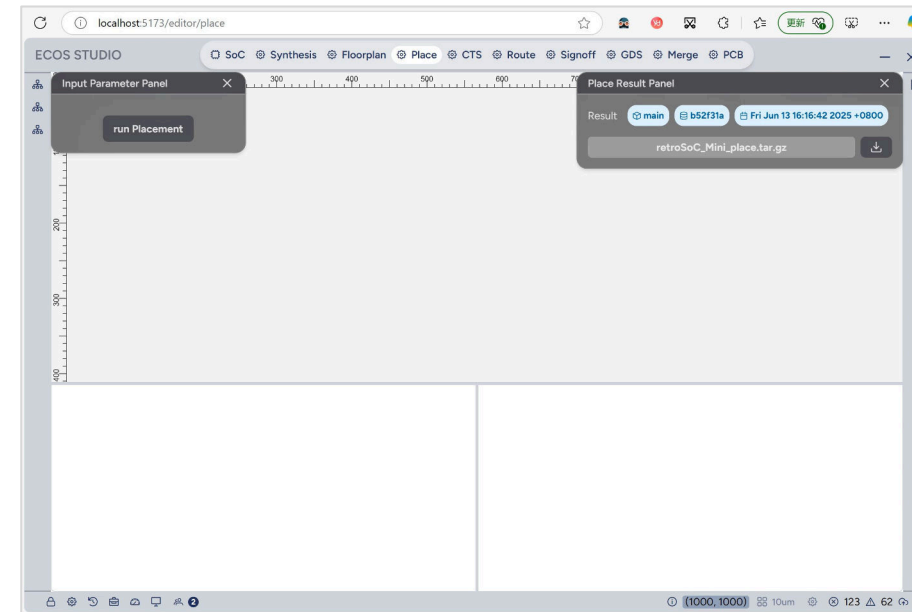
1. start process
2. display reports
3. show congestion

Run CTS

1. start process
2. show animation
3. highlight buffers

Show DRC

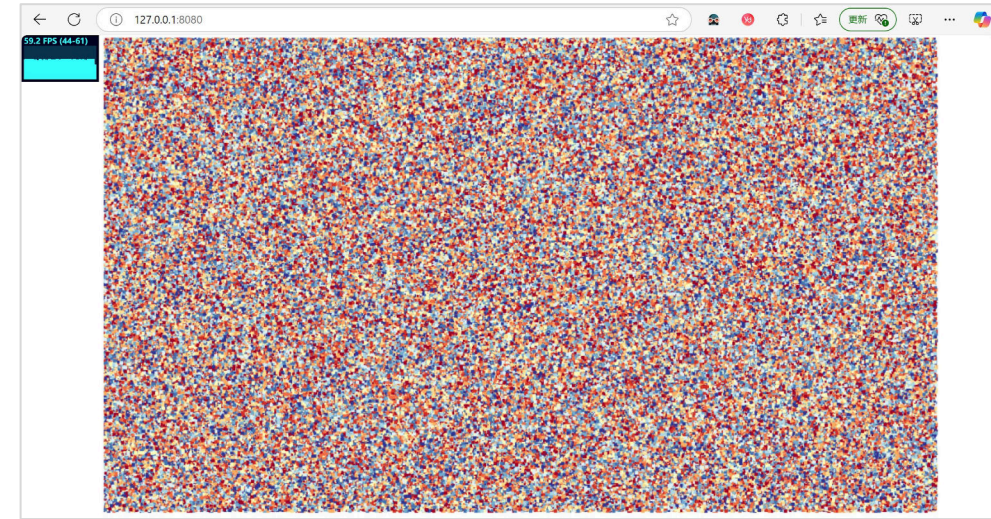
1. start process
2. display DEF file
3. show DRC marks



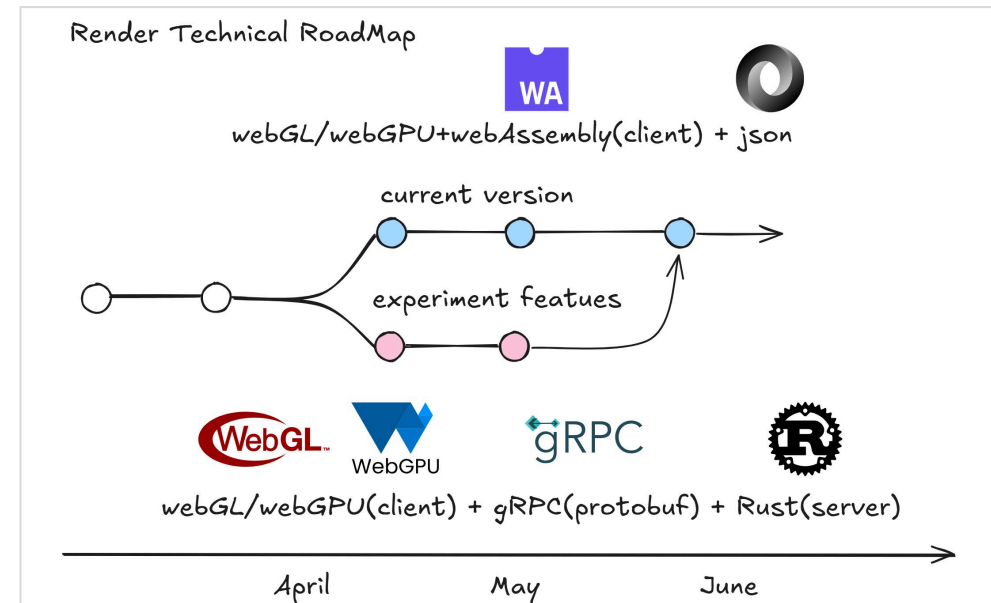
Demonstrate physical design process provided by an undergrad from **One Student One Chip Initiative** (design: single-cycle processor, ~3000 cells in IHP130)

Render Engine of ECOS Studio: AXLE

- **AXLE: *Advanced eXtensible Layout Editor***
 - **key component** of ECOS Studio
 - support **DEF**, highlight/multilayer operations
- Performance evaluation
 - offline rendering (**webGPU backend**)
 - **3M** graphic items(**~60K** gates), render 4 layers(**4/11**)
 - consume **3GB** memory, **800M** GPU, **~30FPS** rate
 - opt. methods: culling, texture cache, offload to GPU
- Technical roadmap (**2025Q3~Q4**)
 - support **LEF/DEF** and **GDS** format
 - support floorplan / powerplan online.
 - improve perf. (support **1M gates**, **<2GB**, **>=25FPS**)
 - webGL/webGPU + gRPC + Rust server
 - integrate/support **Ngspice** simulator

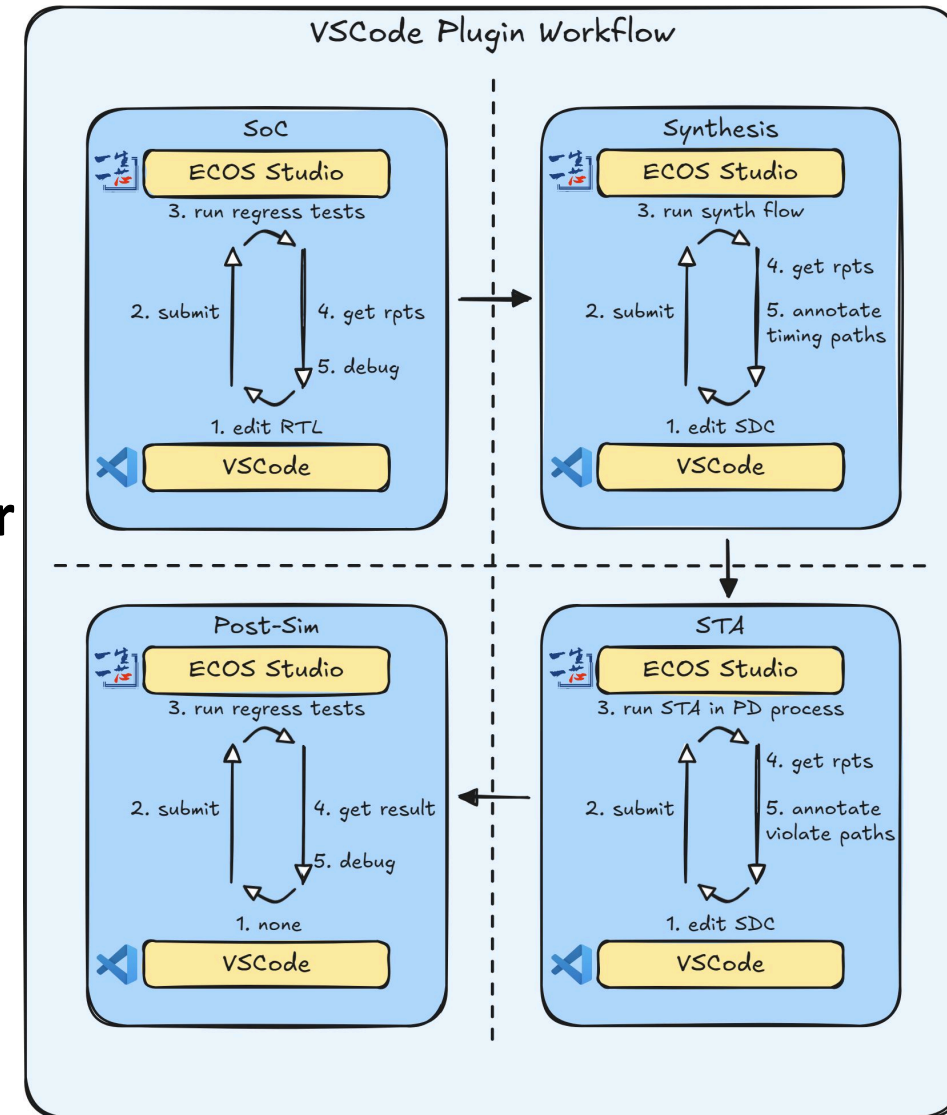


3M Graphic Items Rendering(perf. evaluation)



ECOS Studio: VS Code Plugin / Client

- develop VSCode plugin (**2026Q2~Q3**)
 - offer better editing experience for users
 - edit/submit codes (RTL, C programs...) to ECOS Studio
- Desktop client of ECOS Studio (**2026Q2~Q4**)
 - support **private** deployment in local network
 - remove limitations of rendering **powered by browser**
 - open more system permission to users
 - customize UI Style (background images/font/skin ...)
 - provide localhost API services (**Serial, USB and Audio**)
 - **optimize** for touch-supported devices(**tablet**)
 - implement specification
 - target platform: Win/MacOS/Linux (**x64**)
 - based on Python + Tarui 2.0 (**Rust**)



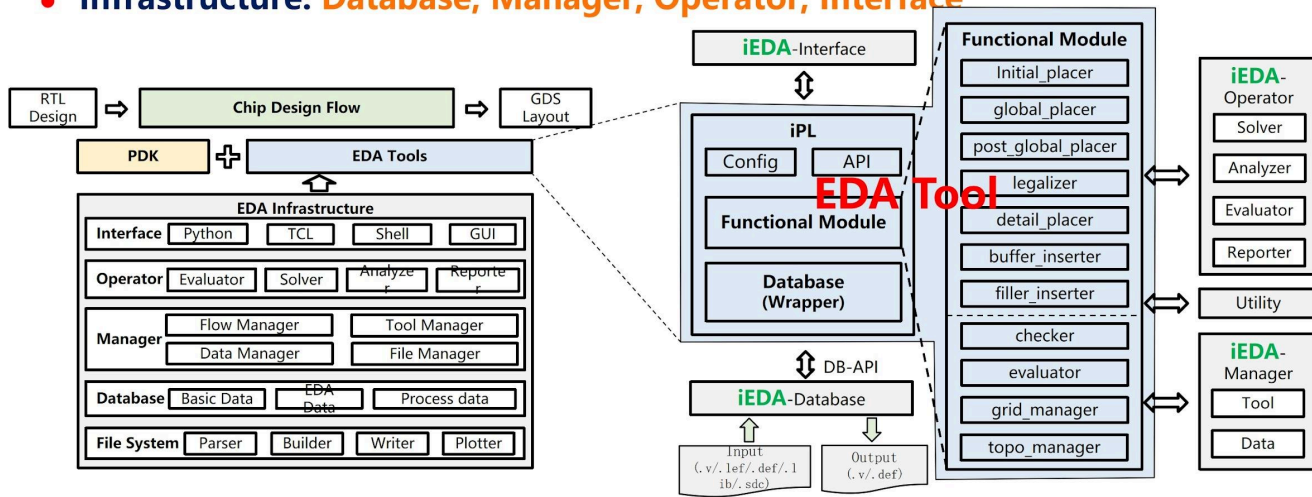
ECOS Studio Engine: iEDA RTL to GDS

- An open-source EDA infrastructure and tools(**start from 2020**)
- **11** sub tools, **400K+** lines code, test tape-out **6** times
 - project: <https://ieda.oscc.cc/en>
 - code: <https://github.com/OSCC-Project/iEDA>
- Develop **ChipCompiler(Flow, support ICS55, IHP/SKY130)**



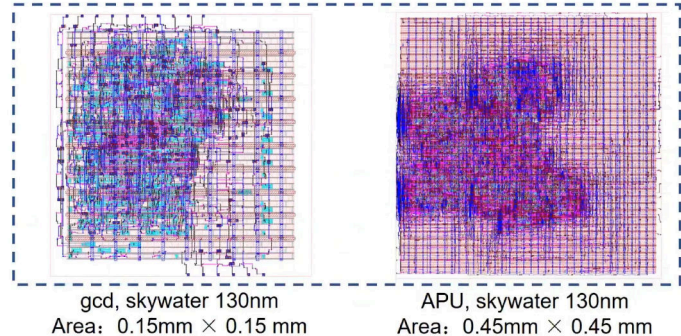
iEDA: Infrastructure

- To fast develop high-quality EDA tool, we need a **Software Development Kit (SDK)**
- iEDA can be used to support developing EDA tool or algorithm
- **Infrastructure: Database, Manager, Operator, Interface**



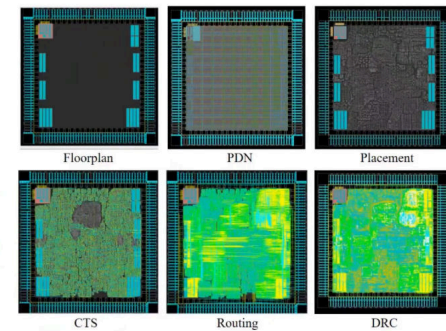
design practice

- gcd & APU



- RTL: ysyx(一生一芯)-04
- PDK: 28nm
- Area: 1.5mm × 1.5 mm
- Power: dynamic = 317mW, leakage = 29 mW
- Freq.: 200MHz
- Scale: >1.5M Gates
- Features: 11 pipelines with cache, IP: UART, VGA, PS/2, SPI, SDRAM, 2 PLLs, support Linux

part metrics	iPL (place)	iCTS	iTO	iRT (route)
#inst	1043440	1057291	1057549	1057549
#net	1015532	1029383	1029641	1029641
utilization	0.563929	0.570644	0.570768	0.570768
HPWL	34108823398	35042653984	35044866877	
STWL	46195026227	46580611921	46581568292	50157263995*
frequency	245.245	238.226	241.386	224.254
#DRC	0	0	0	233335

^a Total wirelength after routing.



iEDA

An open-source EDA infrastructure and tools from Netlist to GDS for ASIC design.

version **1.0.0** mode **>=23.12.01** license **MulanPSL2**

 Watchers 5  Stars 372  Forks 43

[Chinese](#) | [English](#)

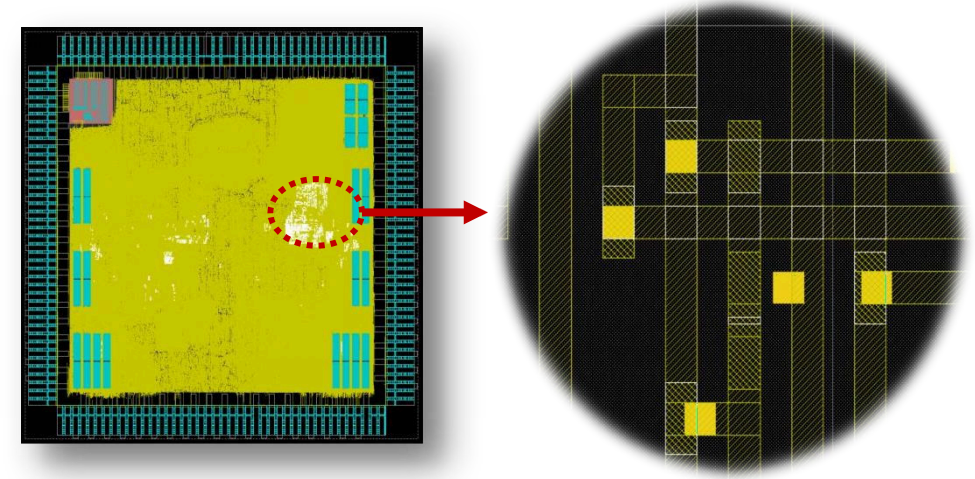
Open-source is not a goal but a way

- **11** tools completed, **5** in active development, **300K** lines code
- well-organized open-source infrastructure supports EDA development and research



iEDA Latest Updates: Enhanced DRC Engine

- Support **ALL DRC Rules** in 28nm node.
- The single-pass **DRC time** is less than 3s in **100K** instances design (routing stage).
- **Compared to Innovus**, the **accuracy** of the major design rules is above **95%**.
- With the **new version of DRC engine**, the **QoR** of **iRT** have been **significantly improved**.



DRC Visualization

Support All DRC Rules in N28:

- Cut Different Layer Spacing
- Cut EOL Spacing
- Cut Enclosure
- Cut Enclosure Edge
- Cut Spacing
- Metal Corner Filling Spacing
- Metal EOL Spacing
- Metal JogToJog Spacing
- Metal Notch Spacing
- Metal Parallel Run Length Spacing
- Metal Short
- MinHole
- MinStep
- Minimal Area

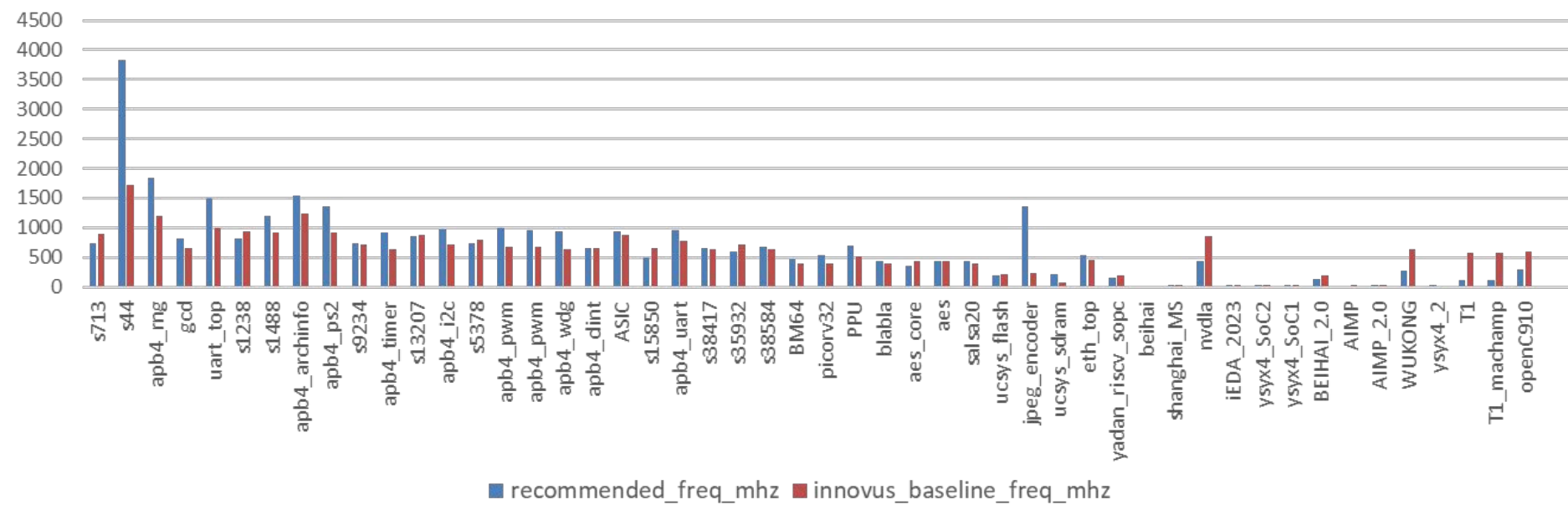
violation_type	correct_num	prop	incorrect_num	prop	missed_num	prop
corner_fill_spacing	39	100.00%	0	0.00%	0	0.00%
cut_eol_spacing	12583	48.55%	6307	24.34%	7025	27.11%
cut_short	163	100.00%	0	0.00%	0	0.00%
different_layer_cut_spacing	6271	99.54%	29	0.46%	0	0.00%
enclosure_edge	1102	82.67%	31	2.33%	200	15.00%
end_of_line_spacing	13867	49.87%	7577	27.25%	6363	22.88%
jog_to_jog_spacing	0	0.00%	0	0.00%	190	100.00%
max_via_stack	0	0.00%	89	50.00%	89	50.00%
metal_short	9422	99.38%	49	0.52%	10	0.11%
min_hole	1048	100.00%	0	0.00%	0	0.00%
min_step	55510	98.63%	384	0.68%	389	0.69%
minimum_area	258642	98.36%	2322	0.88%	1988	0.76%
nonsufficient_metal_overlap	273	100.00%	0	0.00%	0	0.00%
notch_spacing	15230	95.49%	360	2.26%	359	2.25%
parallel_run_length_spacing	23067	97.34%	339	1.43%	291	1.23%
same_layer_cut_spacing	31265	99.99%	3	0.01%	0	0.00%
Total	428484	92.57%	17490	3.78%	16904	3.65%

Compared to Innovus in N28

iEDA Latest Updates: Enhanced Timing Opt. Flow

- Exploring **differentiable timing-driven placement**, **path-based buffering** and **sensitivity-guided gate sizing**, etc.
- We used **50** datasets, ranging in size from **10K to 4M**.
- Comparing our suggest freq. results with Innovus's, **35+ cases** show **closed performance** to Innovus.

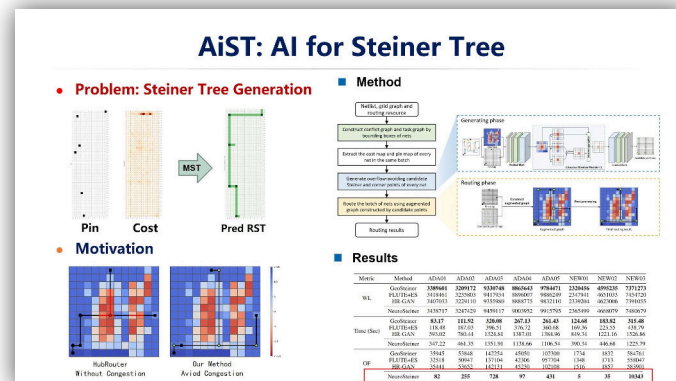
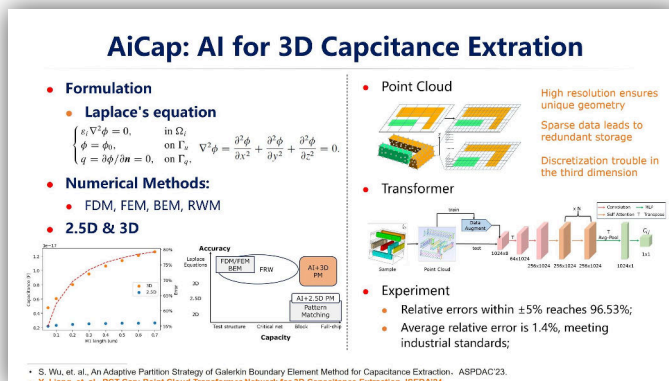
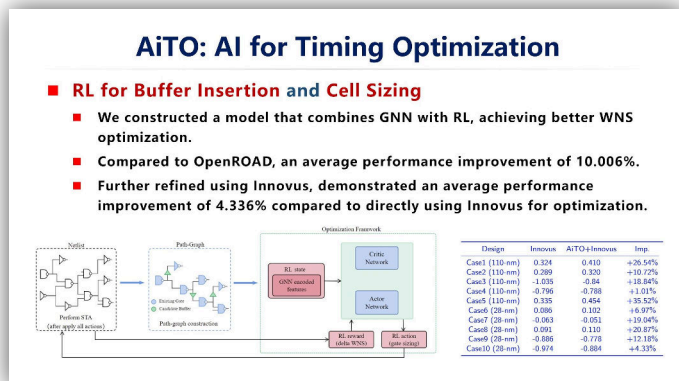
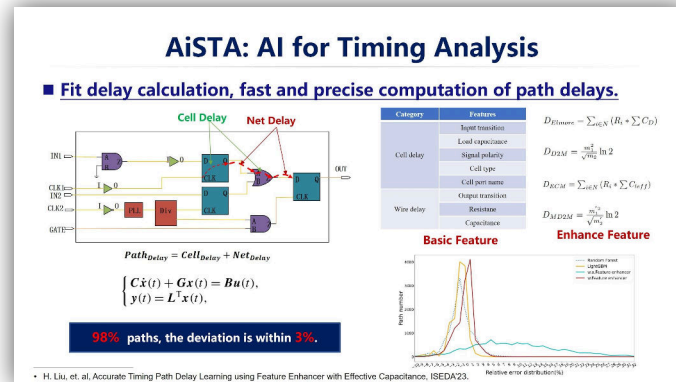
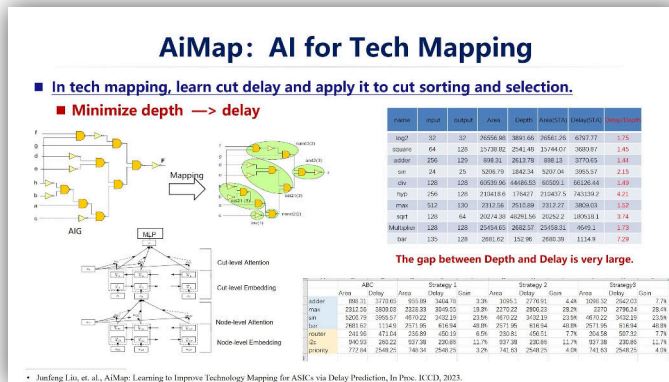
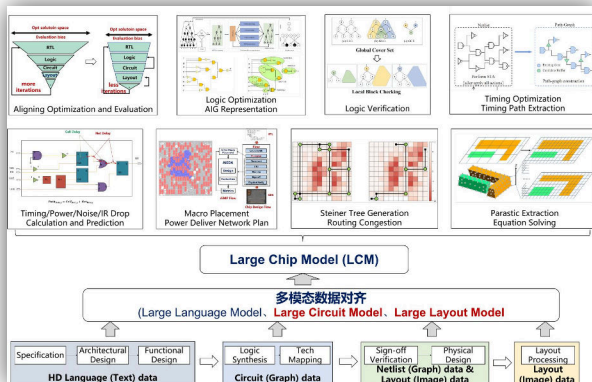
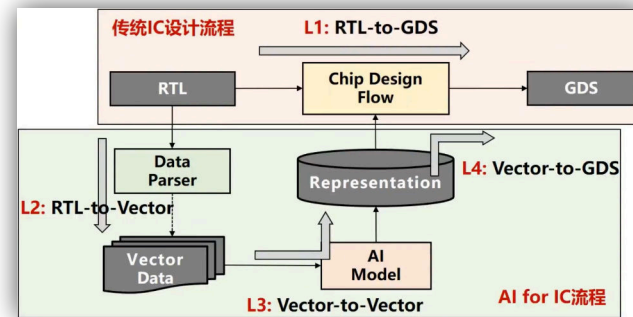
Suggest frequency compared to Innovus



Design_name	Cells	Nets	Wires
s713	135	125	1426
s44	178	128	2095
apb4_rng	195	204	2230
gcd	297	270	3733
s1238	349	290	4998
s1488	380	325	6422
apb4_archinfo	392	381	5122
apb4_ps2	515	497	6542
s9234	657	585	8592
apb4_timer	721	689	8960
s13207	727	647	8182
apb4_i2c	790	727	10248
s5378	881	774	12422
apb4_pwm	974	889	13596
apb4_wdg	1029	945	13889
apb4_clint	1069	1004	13634
ASIC	1228	796	10737
s15850	2088	1926	27941
apb4_uart	5981	5606	83268
s38417	6028	5573	85054
s35932	6375	5837	81158
s38584	7023	6586	97771
BM64	9358	9510	132076
picorv32	9430	9077	136455
PPU	9547	8895	140136
blabla	15154	15672	216427
aes_core	17940	17371	310215
aes	19181	18117	325550
salsa20	21270	20432	291172
jpeg_encoder	27671	29160	366397
retrosoc_asic_cx	30000	30000	30000
eth_top	42279	38552	646875
yadan_riscv_socp	63514	31280	483369
beihai	211236	133086	2161829
shanghai_MS	268721	251772	3610024
nvlla	289344	226974	3708427
iEDA_2023	368147	335112	5132004
ysyx4_SoC2	494962	449847	6967779
ysyx4_SoC1	494962	449847	6967779
BEIHAI_2.0	582645	393308	5491501
AIMP	742210	535618	9980714
AIMP_2.0	816677	560525	9133333
ysyx6	1090820	1029515	15486068
WUKONG	1102663	1032718	15653639
ysyx4_2	1173610	1147953	17416249
T1	1262053	1227098	18769036
T1_machamp	2222669	2162147	33115508
nanhu-G	2793215	2646672	42524007
openC910	3282828	2948743	52259408
T1_sandlash	4816399	4728816	79050737

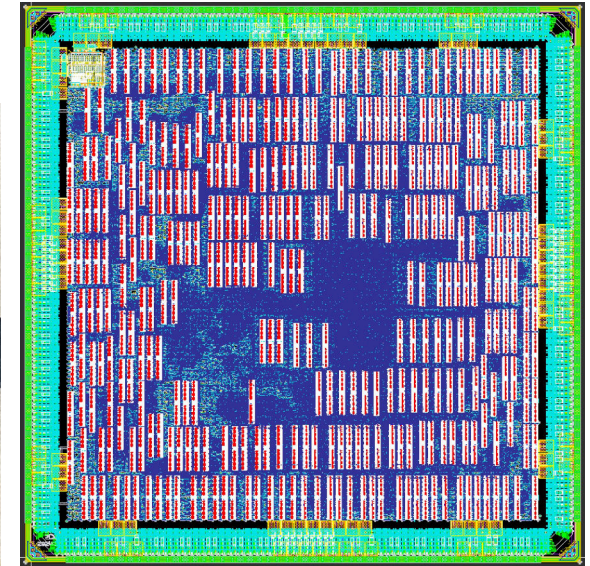
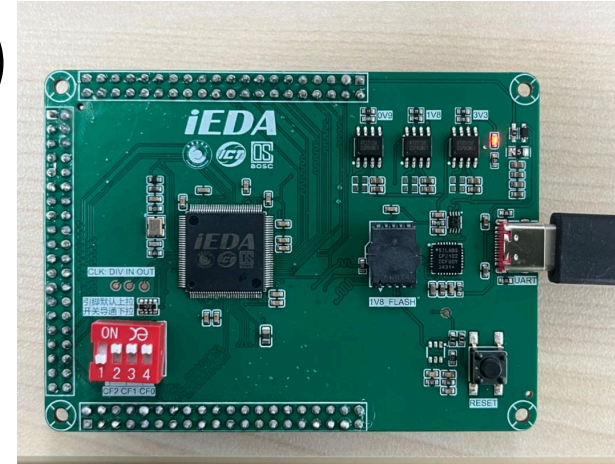
iEDA Latest Updates: AiEDA RTL to Vector to GDS

- AI framework/toolbox in EDA/IC field (**start from 2023**)
- **AI-aided Design (AAD):** RTL2Vec -> Vec2Vec -> Vec2GDS 
- Training **Large Chip Model (LCM)** from iBM, release **AiMap**, **AiSTA**, **AiTO**, **AiCap** and **AiST** models (DAC, ICCAD, ICCD)

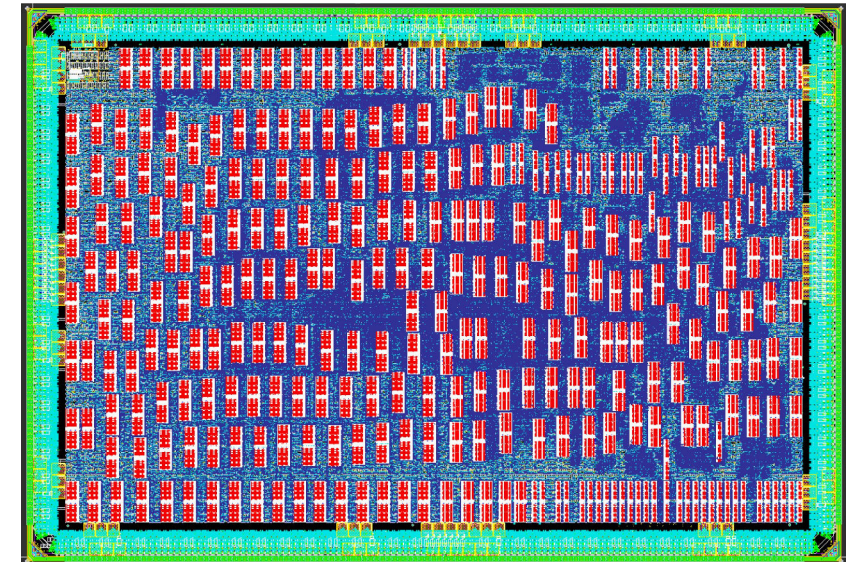


iEDA Latest Tape-out: with AiMP

- “Nutshell”(processor written in Chisel)
 - RV64IMACZicsr, 9-stage pipeline
 - 32KB L1 \$ + 256KB L2 \$ + MMU + TLB
- SoC architecture/design
 - IPs: UART, SPI Flash, SiFive@ChipLink
 - **Single** clock/power domain, **LQFP144**
- Verify macro auto-place with **AiMP** tool
 - Tech Node: N28
 - Floorplan size: 3999.94um x 2700um
 - Utilization: 51.3%
 - Frequency: 900MHz
 - Gate count: **10.49M** Total instance: **0.28M**
 - Power: 334mW Leakage power: 105mW



Tapeout with iEDA and AiMP in N28(2024.8), bring up successfully(2025.2)



Tapeout with iEDA and AiMP in N28(2024.11)
(10M+ gates)

A NEW Open PDK in China: ICSprout 55nm

- ICSprout Semicond. is a **Chinese** foundry (**founded in 2021**)

- jointly established by Zhejiang Provincial Government and ZJU
- have **advanced** 12-inch CMOS 180/55nm process lines
 - 55nm-CMOS, 55nm-eFlash, 180nm-BCD
 - collaborate with universities, academia and industry in China

- open its 55nm-CMOS PDK in **July, 2025**

- MPW tape-out cost (**55nm CMOS Open PDK**)

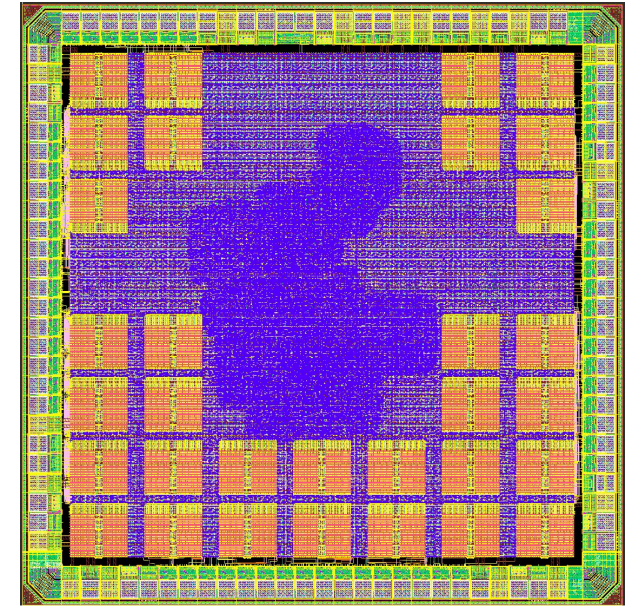
- **Independent:** 30~40K yuan/mm² (\$4,182~\$5,576/mm²)
- **Full Mask (600mm²):** 10K yuan/mm² (\$1,395/mm²)

- Bring ICSprout 55nm Open PDK into **ECOS Studio**

- establish strong cooperation with ICSprout (**What've we done**):

- port our designs and backend flows into ICSprout 55nm Open PDK
- tape-out **FIRST** test chip on ICSprout 55nm Open PDK in **June 15, 2025**
- help to try PD flow and give feedbacks to ICSprout for bugs fixing

develop **OPEN-SOURCE PLL** and **DDR3 PHY** based on ICSprout 55nm Open PDK(**ongoing**)



Design: A RV32IMAC SoC(PSRAM, QSPI, UART, I2C, PWM, TIMER, RNG). **Impl. by Innvovs**
Size: 4mm²(128KB OCM, no PLL)
Freq: 100MHz(external clock bypass)
Gates: 1.517M(73,009 cells)
Power: 115.4mW(dynamic) 0.42mW(static)

iEDA Latest Updates: ICSprout 55nm PDK Support

- We attempted to design a SoC (60K instances, from OSOC) on ICSprout 55nm technology
- DRC clean can be achieved on all metal layers except M1 and timing can approach convergence

	MetSpc	Short	CShort	Totals
MET1	42777	1069	0	43846
MET2	1	0	0	1
VIA2	0	0	1	1
Totals	42778	1069	1	43848

End Verify DRC (CPU: 0.00, 10.2, ELAPSED TIME: 1

The number of DRC

```
zhuangchunan@10:13:40 /mnt/share/home/zhuangchunan/proj/Flow_CX55/bes_data/sta/rpt
^O^ cat retrosoc_asic_VFINAL_1_CTS_TYP_TYP/retrosoc_asic.qor_summary.rpt

Version 2.05

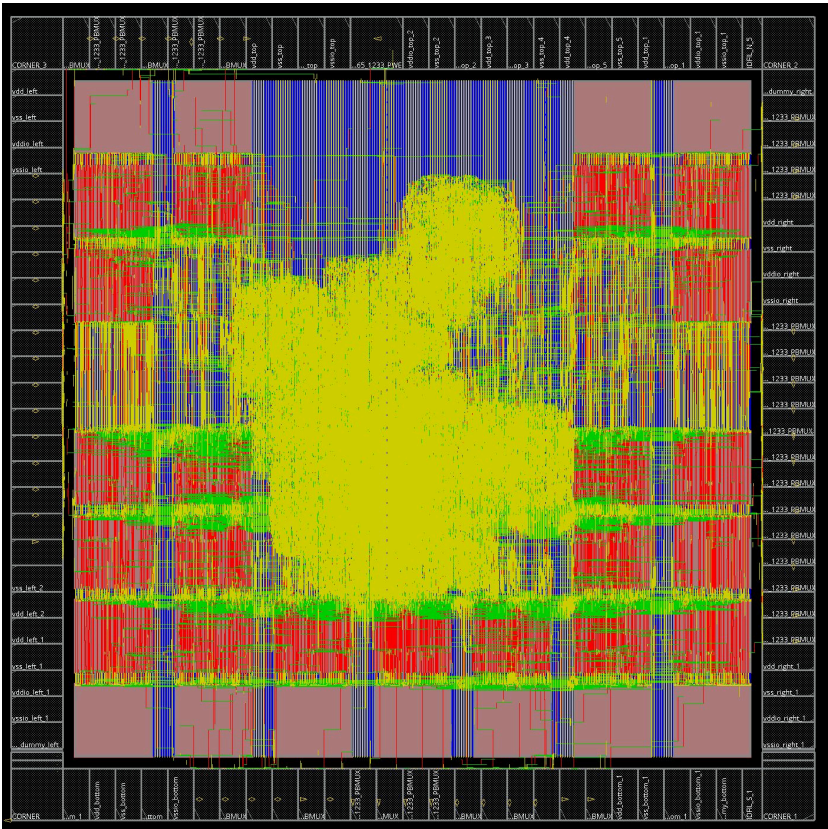
Running report_qor -pba_mode none ; report_qor -pba_mode none -summary ... Done

NVP      - No. of Violating Paths
FREQ     - Estimated Frequency, not accurate in some cases, multi/half-cycle, etc
WNS(H)   - Hold WNS
TNS(H)   - Hold TNS
NVP(H)   - Hold NVP

Path Group      WNS      TNS      NVP      FREQ      WNS(H)      TNS(H)      NVP(H)
-----
CLK_sys_clk_buf  2.390      0.0      0      131MHz    -0.429     -53.3      643
**async_default** 7.445      0.0      0      391MHz     0.060      0.0       0
-----
Summary         2.390      0.0      0      131MHz    -0.429     -53.3      643
-----
CAP  FANOUT  TRAN  TDRC    CELLA  BUFS    LEAFS    TNETS    CTBUF    REGS
-----
292    0    4115  4407   1697601  ~K    35K      ~K      ~      ~
-----
#Union TNS/NVP not found in report_qor, Summary line will report pessimistic summation TNS/NVP
Written qor.csv

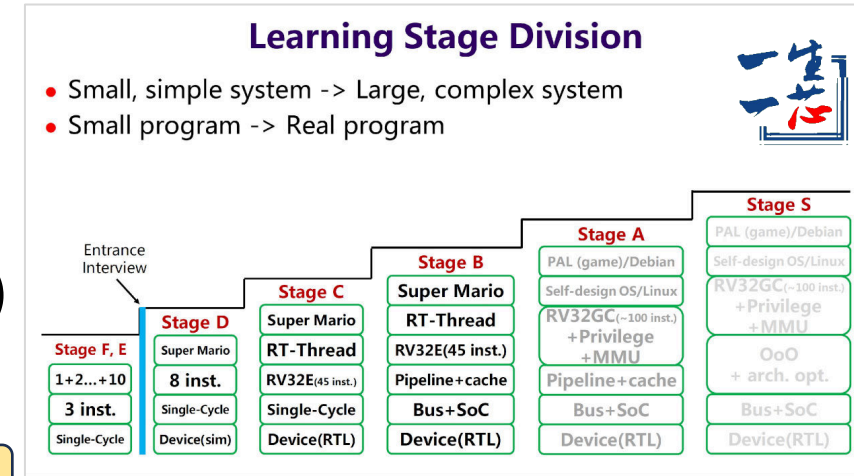
Starting Histogram (proc_histogram) 1.11

Acquiring GBA Endpoints (Slack < 0.0) - ignores REGOUT ...
No Violations or Not enough Violations Found
```



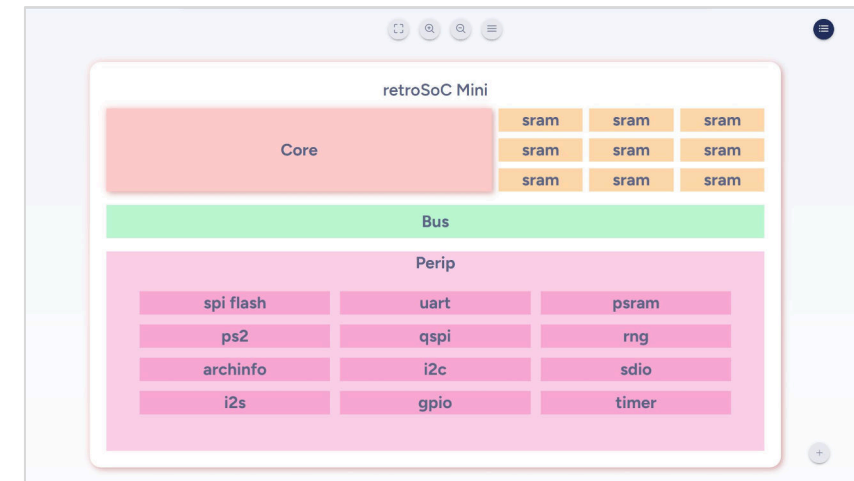
How to bring users to ECOS Studio/ICS55 PDK

- For students from *One Student One Chip*
 - tape-out a single-cycle processor in *Stage D*
 - complete HW/SW, pass online assessment (**OSOC tutorial**)
 - complete PD flow, merge design to SoC template (**ECOS Studio**)
 - design is very small
 - impl. **8 instructions + axi4l**, can run “*Super Mario*”
 - **~3848 cells, 0.011mm²** in ICS55, DRC num < 10, **~100 yuan(\$14)**
 - tape-out **FOR FREE** (for Chinese students)
 - design tutorials, labs based on ECOS Studio and ICS55 PDK
 - help **200+** undergrads to **tape-out in ICS55** later this year



Later, we'll give a brief introduction

- For academia or individual (**2026Q2~Q3**)
 - support online SoC integration (**powered by IP Market**)
 - open source **PLL** and **DDR3 PHY** IP on ECOS Studio
 - allow users to upload verified EDA algorithm to evaluate
 - provide flexible sales mixes (**Independent/Multi-Die**)

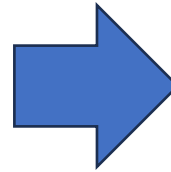


“SoC Canvas”
(SoC design component of ECOS Studio)

Open Silicon Design Course – Using ECOS Studio

“One Student One Chip” (start from 2021.6)

- Teach students to design **real chips** in **open PDK**
- Focus on promoting students’ professional abilities
- Content (**real full-stack!**)
 - HW/SW co-design (**APP, simulator, runtime, OS, micro-architecture**)
 - logical/physical design (**formal, synthesis, PPA evaluation, RTL2GDS flow**)
- Feature
 - Infrastructure (**AM, NEMU, CacheSim/BrSim, DiffTest, SDB, SymbiYosys, Yosys, iEDA...**)
 - extensive teaching experience (**involved 12000+ students**)
 - **tape-out for free!** (students who pass the online assessment)
- New version with **open EDA & PDK** will release in **2025** soon



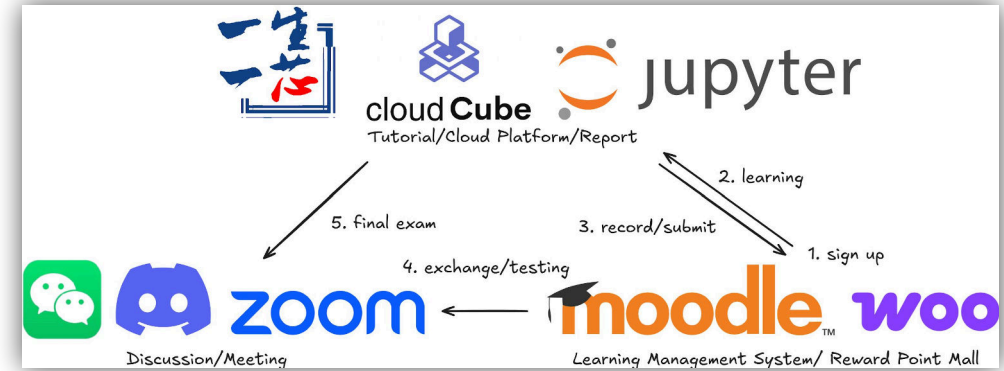
Open silicon design course (will start from 2025.9)

- Teach students to complete SoC & physical design with **open EDA** in **ICS55** powered by **ECOS Studio**
- **Fill the gap** between academic and industry
- Content
 - transistor circuit (**gate structure/simulation**)
 - SoC design/integration/verification (**CDC, UVM, STA, TCL, SDC...**)
 - physical design (**whole backend flow**)
- Feature
 - Infrastructure (**xschem, ngspice, KLayout, Cocotb, pyUVM, Yosys, iEDA, OpenROAD, cloud platform...**)
 - establish open, flexible and **community-driven** teaching-learning mode
 - tape-out in **ICS55** with iEDA on ECOS Studio
- Release first version in **2025Q3**

Today we are HERE!

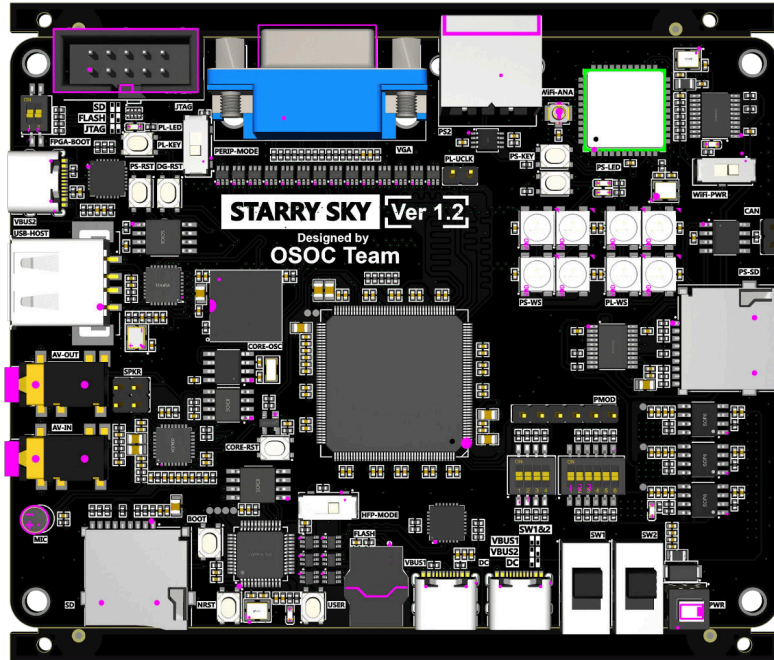
Open Silicon Design Course

- Using complete open-source toolchain
 - xschem, ngspice, Klayout (**Transistor**)
 - cocotb, pyuvvm, SymbiYosys (**SoC**)
 - Yosys, OpenROAD, ICS55 open PDK (**Physical design**)
 - **self-developed tools**: HDLVim, teenySoC, ACES, AXLE, iEDA, **ECOS Studio** (ongoing) ...
 - ...
- Developing **LMS-Centric** website (servers are located in **Hong Kong SAR**)
 - have unified ID verification and modern UI system
 - customize an extensible, robust and easy-to-use **LMS** and **Reward Point Mall**
 - put all handout, webinar video, slides, tools, contest/marathon... **in one place!**
- More open and professional **learning support**
 - encourage rapid discussion on WeChat/Discord
 - 5~10 full-time TAs with 6~7 volunteers

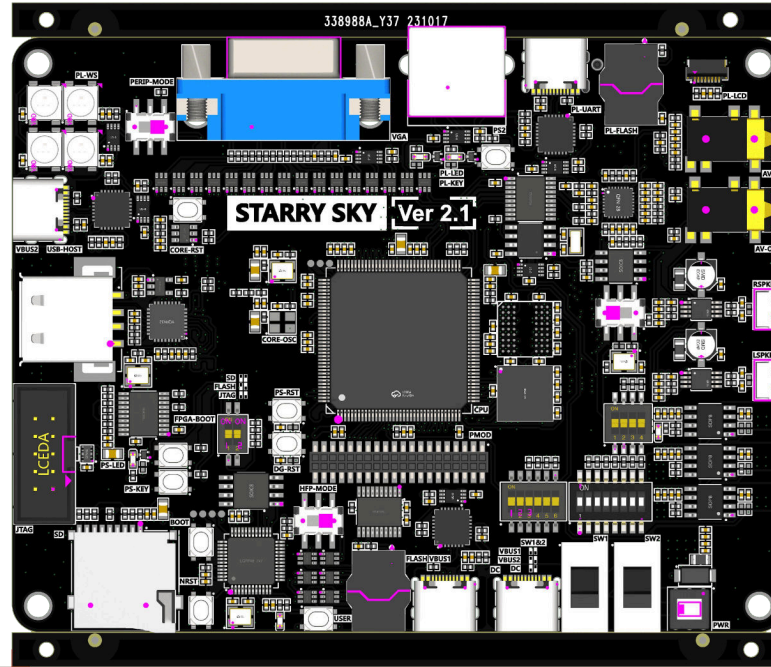


Post-silicon Education in 2025Q4/2026Q1

- Provide **post-silicon education in future**(bonding/packaging, PCB, bring-up, ...)
- **Shorten** development period(SDK, APP, software, product packaging ...)



- solder OSOC 3rd chip(**110nm**)
- **6-layers** stack design(Allegro)
- officially release in **2023.4**



- solder OSOC 4th chip(**28nm**)
- **8-layers** stack design(Allegro)
- officially release in **2023.10**

What's next?

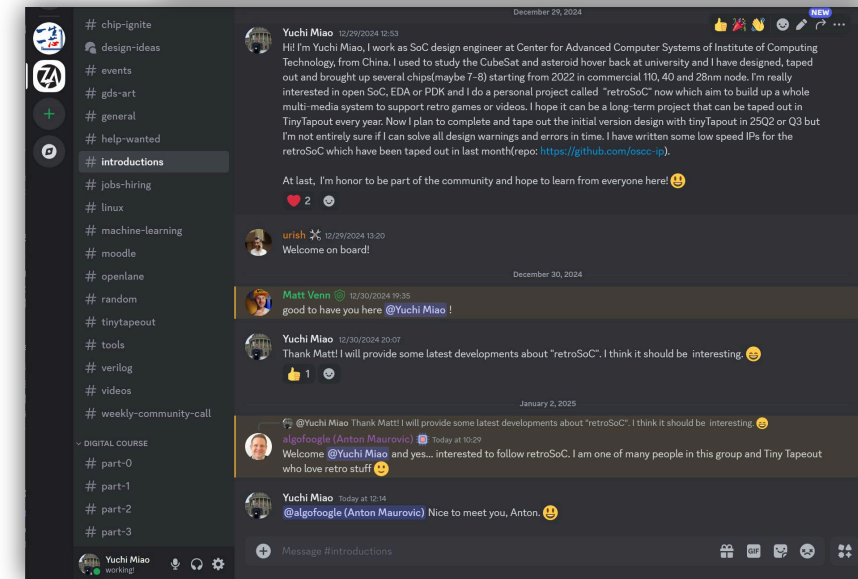
1. platformized, componentized
2. encourage MORE students involved!

- solder OSOC 5th chip(**28nm**)
- **4-8 layers** stack design(KiCad)
- coming soon! expected in **2025.7**

Design Practices: A Customized ASIC retroSoC

- An open source SoC framework(**maybe ~5 years that all can be done**)
 - generated by **ACES**(Rust SoC builder, using “Combo” config)
 - provide WiFi, MIPI, ISP, 2D/3D graphic accelerator(**ongoing**)...
- Focus on some stuff:
 - **retro game console**
 - **APS-C/full-frame CMOS camera**
 - ...
- Build up a **community-driven** develop mode
 - get instant feedbacks **in super early stages**
 - make continued influence
- Provide **baseline** for iEDA, AiEDA and openROAD
- Tape-out a **real chip** by using open PDK
 - long-term project
 - supported by community(**ECOS Studio**, Tiny Tapeout ...)

apertus AXIOM BETA Compact



retroSoC: Technical Roadmap in 2025

- A MCU-class **RV32IMAC** SoC(~50K instances, demo: **smart watch**)(2025Q3)
- An Application-class **RV64IMAC** SoC(~100K instances, demo: **game console**)(2025Q4)

MINI

1. RV32I/EC
2. minimum design
3. no on-chip SRAM
4. wrote in Verilog
5. 10~20K instances
6. package: QFN48/64
7. demo: smart band

STD

1. RV32IMAC
2. balance design
3. ITCM/DTCM/Cache
4. wrote in SV
5. 30~50K instances
6. package: QFN88
7. demo: smart watch

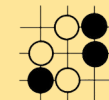
PRO

1. RV64IMAC
2. high-performance
3. L1/L2 Cache
4. wrote in SV
5. 50~100K instances
6. package: QFP100
7. demo: boot Linux

Major milestone

1. harden design(**MDD**)
2. maintain the CRT
3. run open EDA CI/CD
4. SoC integrate, design, verification(**key point**)
5. run commercial flow
6. write dev./use guide
7. switch to iterative dev. mode
8. auto-generated by SoC builder(**teenySoC**)

1. Low-speed IPs: UART, TIMER, PWM, WDG, RTC, I2C, SPI, PS2, RNG, ...
2. Memory IPs: QPI PSRAM, OPI DDR PSRAM
3. Application IPs: SDIO, DMA, VGA, DVP, USB1.1, I2S, 2D Graphic Accel.



clusterIP

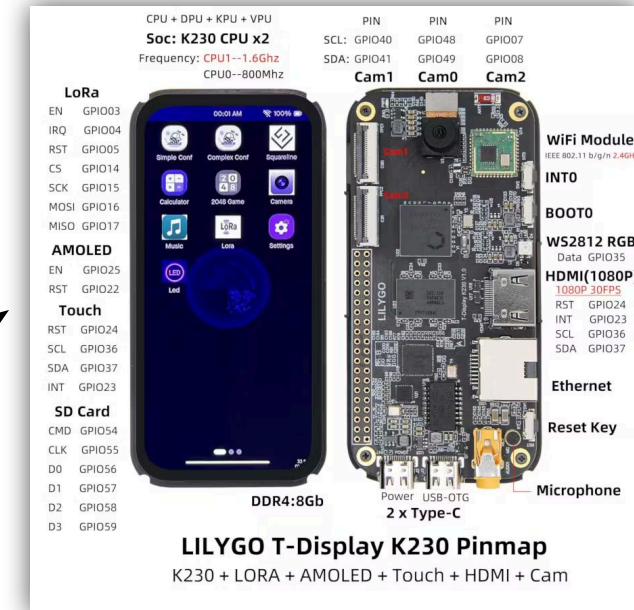
retroSoC: Multimedia IPs Development Plan

- A community-driven project(**hosted by OSOC Shenzhen Base**)
 - led by internal **special R&D group**(composed of TAs and interns)
 - develop DMA, SDIO, DVP, USB, 2D Graphic Accel. etc.
 - **full-stack design**(IP, SoC, SW, PCB, Pack., Docs)



<https://github.com/retroSoC>

MEM		QPI PSRAM				OPI DDR PSRAM		
HW	SPI DMA	SDIO	I2S	VGA/LCD	DVP	USB1.1(ULPI)	2D GRAPHIC ACCEL.	
SW	TFT-LCD	Video/WiFi	Audio/Game		Camera	Disk/Mouse/KBD.	Graphic API	
SoC		MINI/STD				STD/PRO		
APP (PCB, PACK., DOC.)								
	2025Q1		2025Q2		2025Q3		2025Q4	



retroSoC: Multimedia IPs Development Plan

- PrismGPU project(<https://github.com/PrismGPU>) →



- a new open-source 3D GPU
- plan to support **FULL** OpenGL 1.x API(MESA)
- first version will be integrated into **retroSoC Pro**
 - optimize for a **Linux-capable** single-core(RV64GC) SoC
 - fix-function pipeline, DMA+AXI+VGA arch.(no video codec impl.)
 - give priority to adapting **Quake**, **Need for Speed III: Hot Pursuit**
 - tape-out in **2025Q4~2026Q1**



- collate and open all learning materials(2026Q2~Q3)
 - tape-out for students in **Stage A or S from One Student One Chip**
 - design a practice-oriented GPU tutorial
 - CG(**GAMES101**) -> Graphics API(**LearnOpenGL**) -> Driver(WDDM)
 - design soft pipeline -> impl. device drivers(**Gallium3D, QEMU**)
-> impl. Linux DRM -> write fix-function pipeline(**Hardware, FPGA**)
 - a tiny GPU implemented by students will be tape-outed



Moving Forwards

- Improve **performance** and **quality** of ECOS Studio
 - provide high-performance render for DEF/GDS(**more interactive operations**)
 - considered as a real product(user needs&experience, design flow, **load/stress test...**)
 - integrate some components of AiEDA and **AI agent(in Floorplan, DRC fix flow)** ...
- Support more foreign students to learn
 - hope >500 students enroll(**~100 complete coursework**) in 2025
 - more infrastructure(translation, easy-to-use LMS, clusters allocation...)
- More involved in **international activities** for **exchanging ideas**~(// '▽' //)
 - webinar, workshops/conferences(**FSiC, Latch-Up, ORConf**) ...
 - poster, essay, paper, talk
- **Redefine** cultural and creative products(Yeah, it must be right!)
 - maybe need a cute **mascot** (// '▽' //)
 - T-shirt, sticker, wristband, wallpaper, meme, photo, short film...
 - more offline activities

ECOS Studio/iEDA Events in 2025

- **Latch-Up 2025(talk)**, Santa Barbara, CA, USA, May 2-4, 2025
- **RISC-V Summit Europe 2025(posters)**, Paris, France, May 12-15, 2025
- **GROW 2025(talk)**, São Paulo, Brazil, June 30-July 2, 2025
- **FSiC 2025(talk)**, IHP, Frankfurt (Oder), Germany, July 2-4, 2025
- **RISC-V Summit China 2025(talk)**, Shanghai, China, July 17-19, 2025

Talk: “RISC-V Chip Design Solution Based on Open-Source IP and Open-Source EDA”, Biwei Xie, Associate Professor, ICT, CAS

ECOS Studio will be first RELEASED here!

Rollout time: **July 16** Website: <https://studio.ecoslab.com>

- **ORConf 2025(plan)**, Valencia, Spain, September 12-14, 2025
- **RISC-V Summit North America 2025(plan)**, Santa Clara, USA, Oct. 22-23, 2025
- **Open Source @Siemens China 2025(talk)**, Wuxi, China, October 30-31, 2025
- **RISC-V Day Tokyo 2025 Autumn(plan)**, Ito Hall, U-Tokyo, Japan, Dec. 4, 2025

Q&A

Xueyan Zhao<zhaoxueyan21b@ict.ac.cn>, Hao Wang<wanghao@ict.ac.cn>
github.com/zhaoxueyan1 github.com/Oxharry

Yuchi Miao<miaoyuchi@ict.ac.cn>
github.com/maksyuki

ECOS Team of Center for Advanced Computer Systems,
Institute of Computing Technology, Chinese Academy of Sciences

Free Silicon Conference 2025 – IHP, Frankfurt (Oder), Germany
July 2-4, 2025

FSiC2025
Free Silicon Conference

