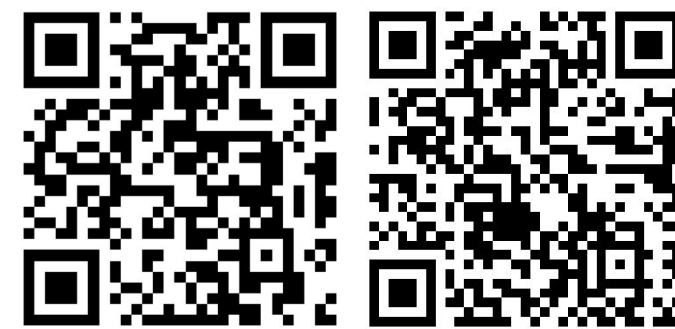




Website: ysyx.org/en Telegram
Email: ysyx@bosc.ac.cn Group

“One Student One Chip” Initiative

Learn to Build RISC-V Chips from Scratch with MOOC

OSOC Team

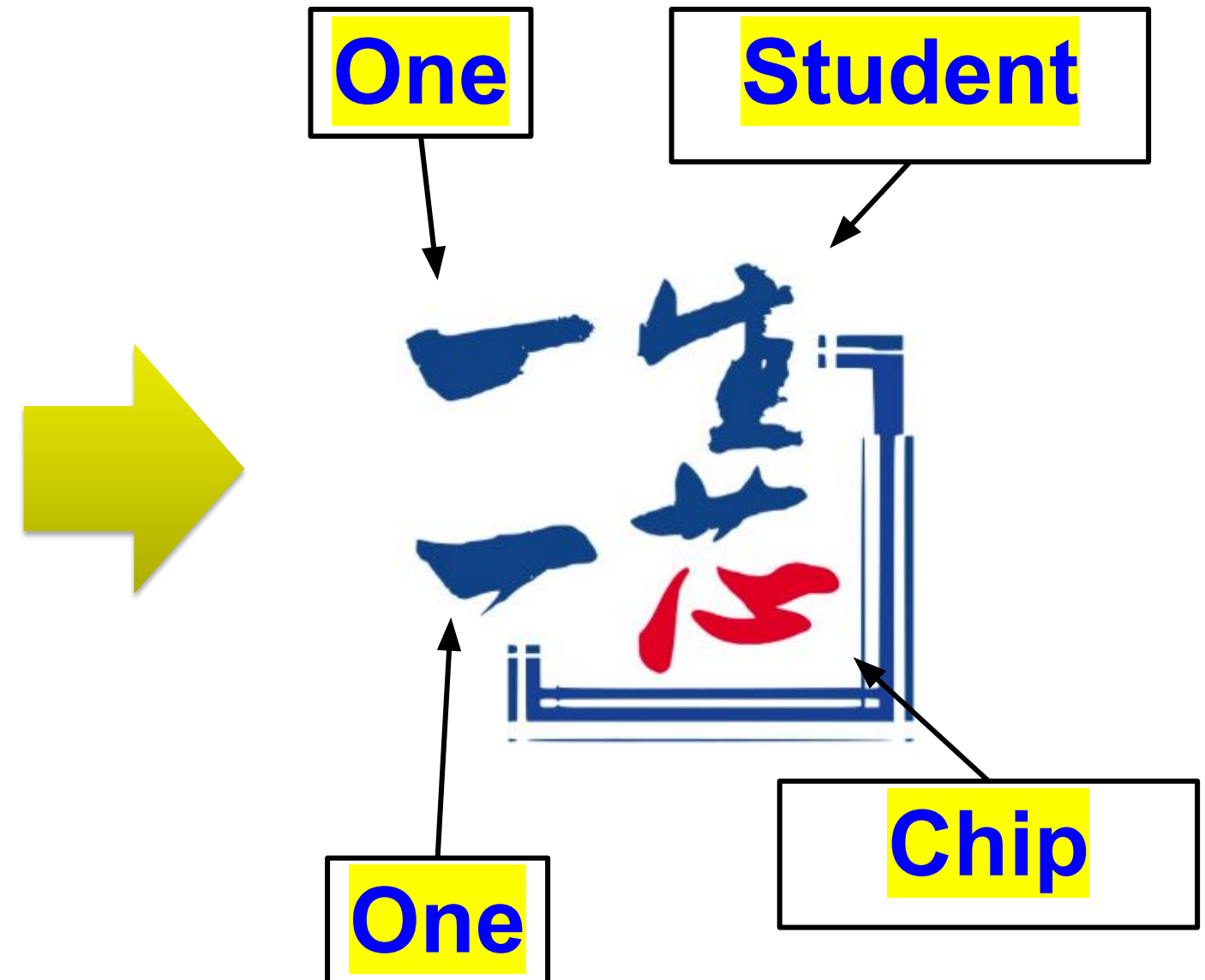
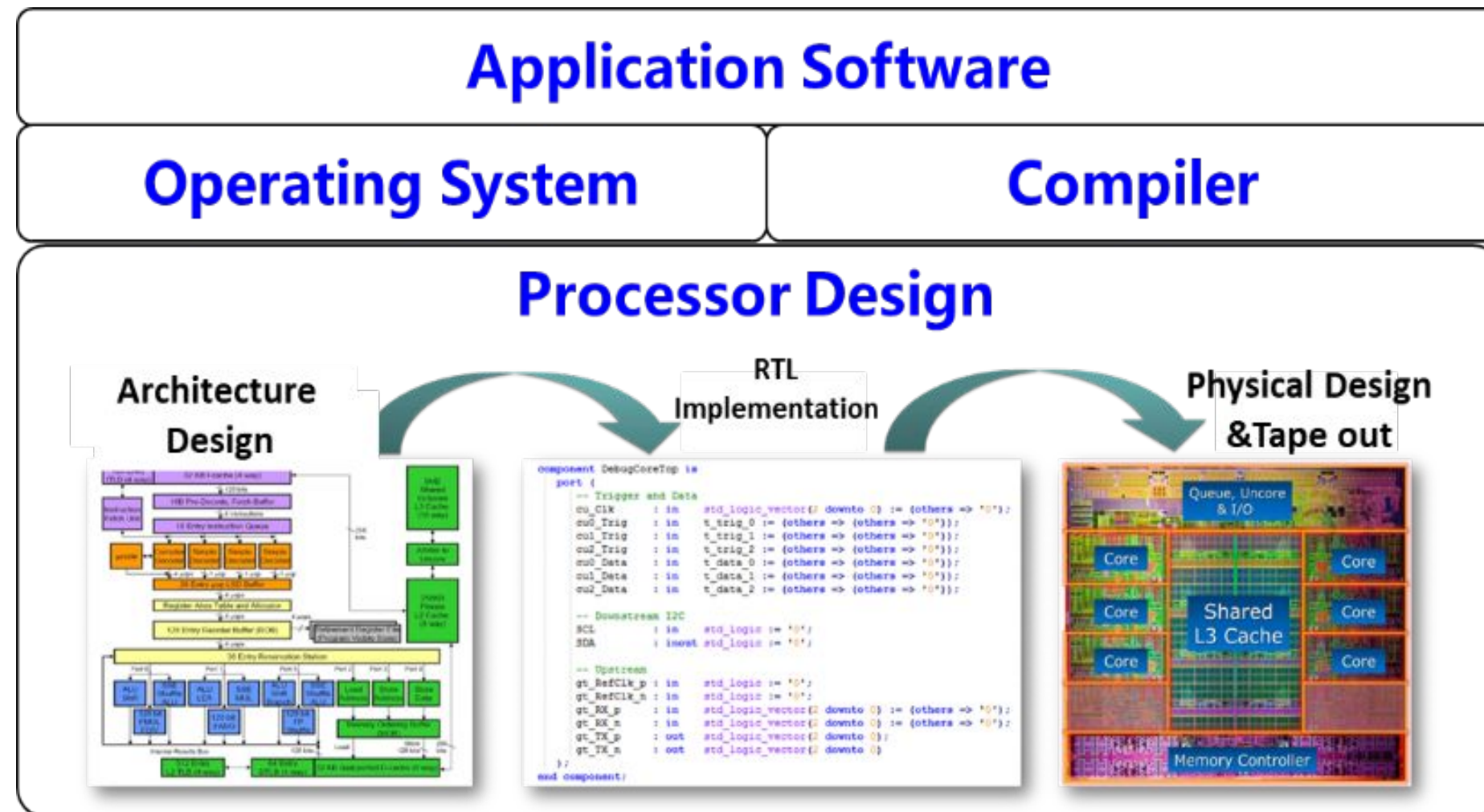
2025. 07



1. Background

The One Student One Chip (OSOC) Initiative

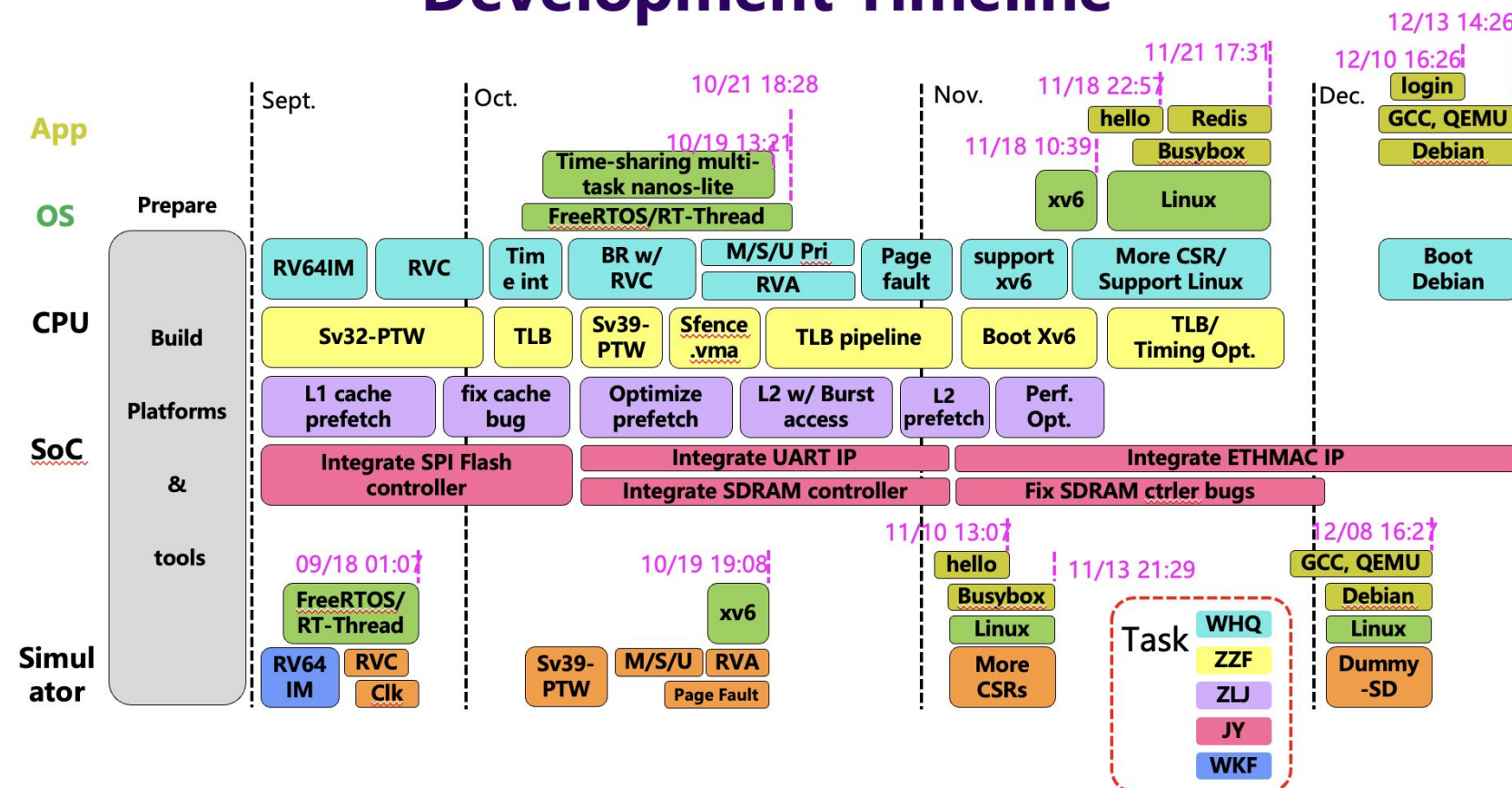
- Launched in 2019 by UCAS (University of Chinese Academy of Sciences)
- **Learning-by-doing** : Teach students to build real chips
- **Non-profit** : Free learning for everyone, free tape-out for students
- **Open** : Everyone is welcomed
- **Learn-on-demand**



The 1st OSOC (Aug to Dec, 2019)

- Allowing a student to graduate with a processor chip designed by herself/himself
- Five senior **undergraduates** of UCAS participated
- Completed the design of **a 64-bit RISC-V** processor in **four months**
- The chip was **taped out** with 110nm and ran Linux and a self-built UCAS-core OS successfully

Development Timeline



1st OSOC finished successfully

- 1st OSOC Goal Achieved!!
- The students of 1st OSOC graduated with their own RISC-V processor chips!



NutShell: A Linux-Compatible RISC-V Processor

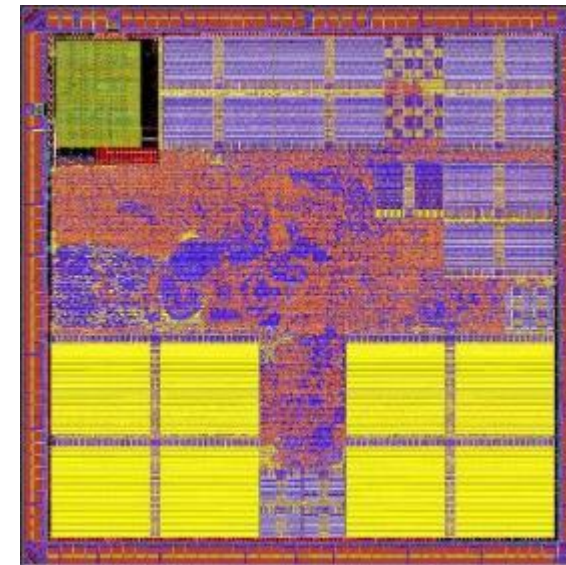
Designed by Undergraduates

(1st OSOC processor chip)

A 64-bit RISC-V Processor

- Single-issue, 9-stage, in-order
- RV64IMAC, support M/S/U
- BPU with PHT, 512-entry BTB, 16-entry RAS
- Sv39, hardware TLB refill
- 32K L1I & L1D
- Read consistency for L1I & L1D
- 128K L2 cache, next line prefetch
- Develop with Chisel
- SDRAM, SPI flash, UART
- Support Linux 4.18.0 kernel
- Support Busybox
- Can boot Debian 11 on Emulator & FPGA

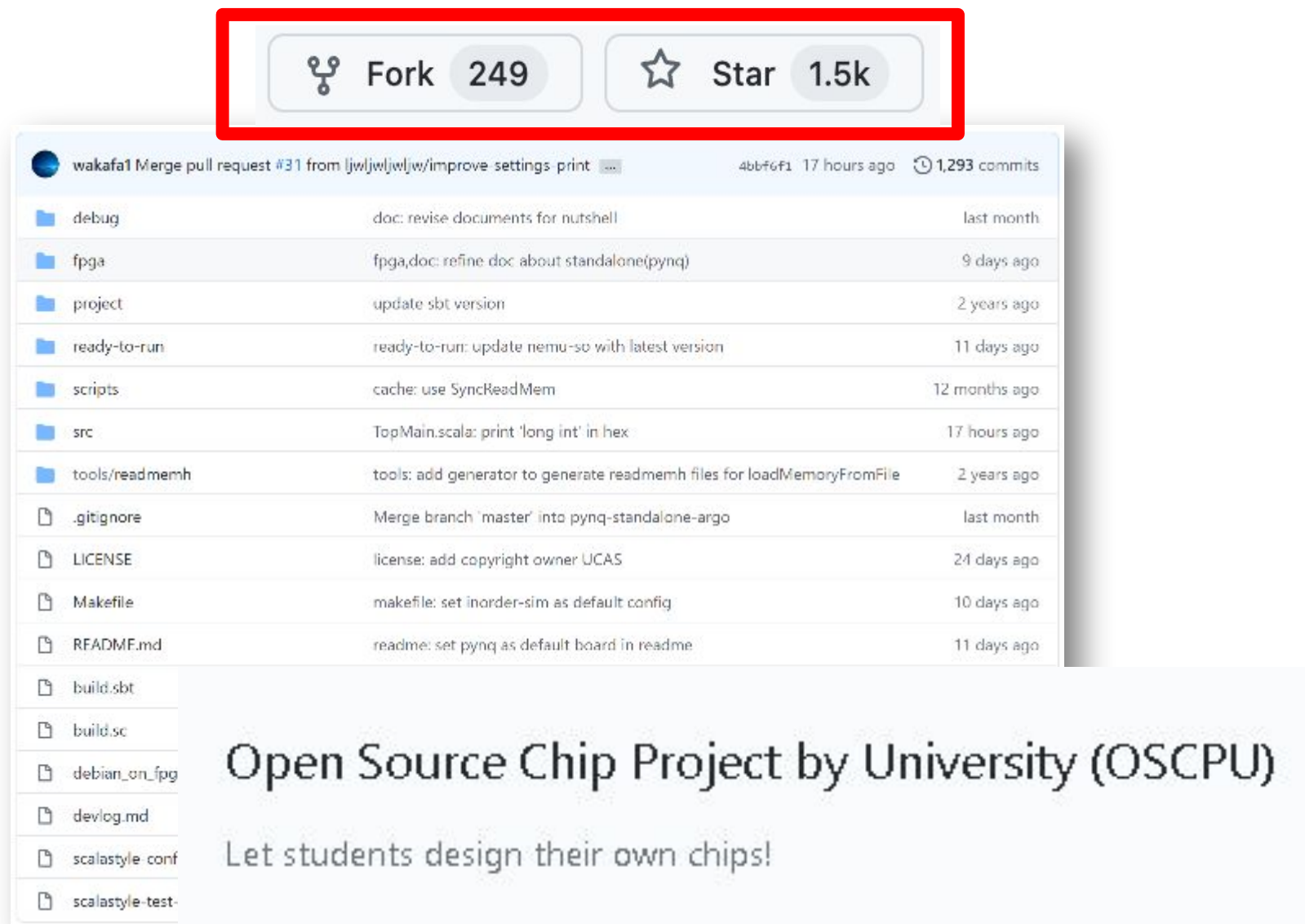
Tape-out w/ 110nm process



- 110nm process
- 10mm²
- 200mw@350MHz Typical
- TQFP100 package

NutShell : Open-sourcing

- Open-sourced on **GitHub**
 - **NutShell : #Fork > 245**
- **OpenEuler, an OS developed by Huawei, is booted successfully on NutShell**



<https://github.com/OSCPU/NutShell>

```
[ 2.680000] clk: Not disabling unused clocks
[ 2.690000] Waiting for root device /dev/mmcblk0p2...
[ 2.760000] mmc0: new high speed SDHC card at address aaaa
[ 2.810000] mmcblk0: mmc0:aaaa S08G 7.40 GiB
[ 2.840000] mmcblk0: p1 p2
[ 2.980000] EXT4-fs (mmcblk0p2): mounted filesystem with ordered data m
[ 2.990000] VFS: Mounted root (ext4 filesystem) on device 179:2.
[ 3.010000] devtmpfs: mounted
[ 3.020000] Freeing unused kernel memory: 176K
[ 3.030000] This architecture does not have kernel memory protection.
[ 4.300000] random: fast init done
[ 6.550000] systemd[1]: System time before build time, advancing clock.
[ 6.630000] systemd[1]: Failed to lookup module alias 'autofs4': Functi
[ 6.910000] systemd[1]: systemd v243-18 running in system mode. (+PAM +
+IDN2 -IDN +PCRE2 default-hierarchy=legacy)
[ 6.940000] systemd[1]: Detected architecture riscv64.

Welcome to openEuler 20.03 (LTS)!

[ 7.040000] systemd[1]: Set hostname to <openEuler-RISCV-rare>.
```

Feedback from students

Self-exploring

The biggest difference compared to previous experiments is that there are **no detailed step-by-step instructions** from predecessors. Instead, I have to **find my own methods, implement them independently**, and then validate the results—even if it means starting over from scratch.

From user to creator

Professor Hu Weiwu once said that as CS students, we should learn how to build computers, not just how to use them. I did not fully appreciate this statement before; in fact, I once questioned whether it was reasonable for the CS curriculum at UCAS to include so much hardware content. However, it was only **after getting involved in real projects that I realized the knowledge and skills learned in university are truly valuable**.

The **working principles** in the architecture course are **straight-forward**, often just a few short lines. However, **implementing them in code turned out to be far more challenging than I had imagined**.

More confidence, more patience

Compared to myself four months ago, **the most significant change is this shift in mindset**. When facing bugs, I no longer stubbornly focus on one point. Instead, I tell myself that bugs are written by people, and as long as **I have patience and dig deep enough, I will definitely find the problem**.

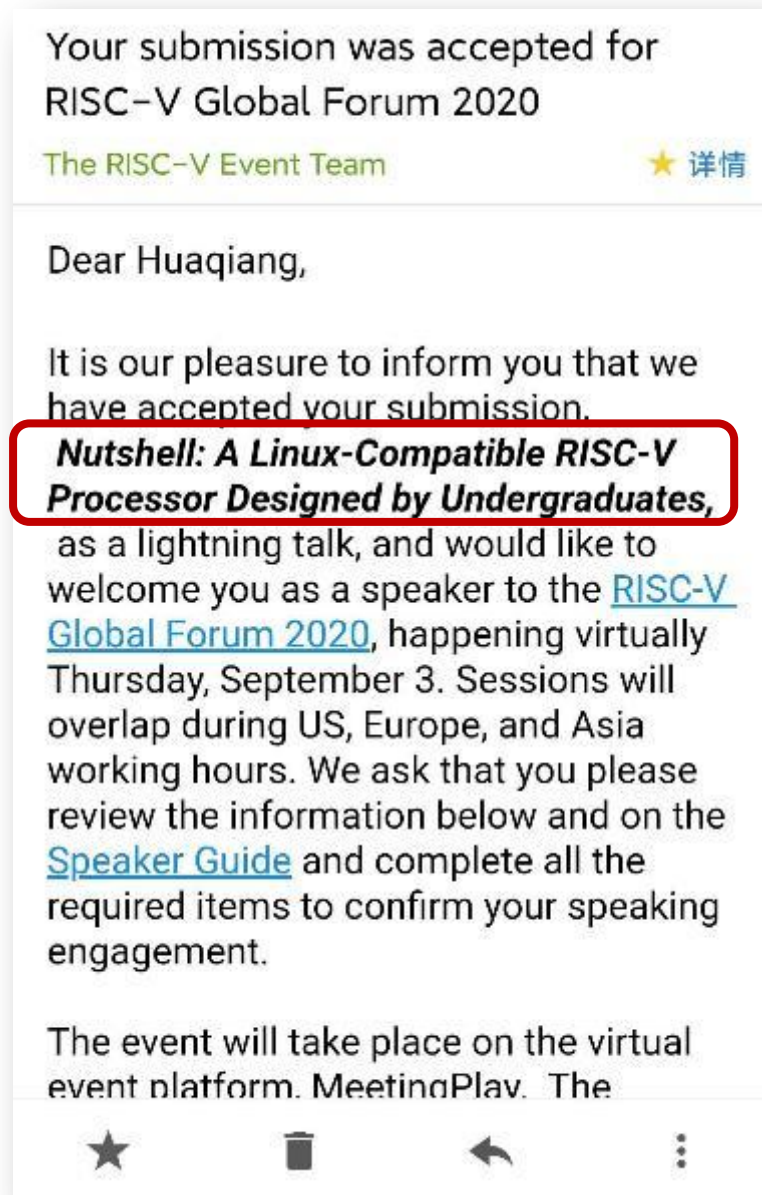
Accomplishment

It was only after getting involved in this project that I realized course assignments are like a ready-made orchard where you simply pick the fruit, whereas a project is more like being **handed a barren piece of land and a few saplings**. You have to do everything yourself—from clearing the ground to planting and fertilizing—without knowing whether the effort will bear fruit. For some reason, **it feels like the fruit grown from scratch tastes sweeter**.

Empower students!

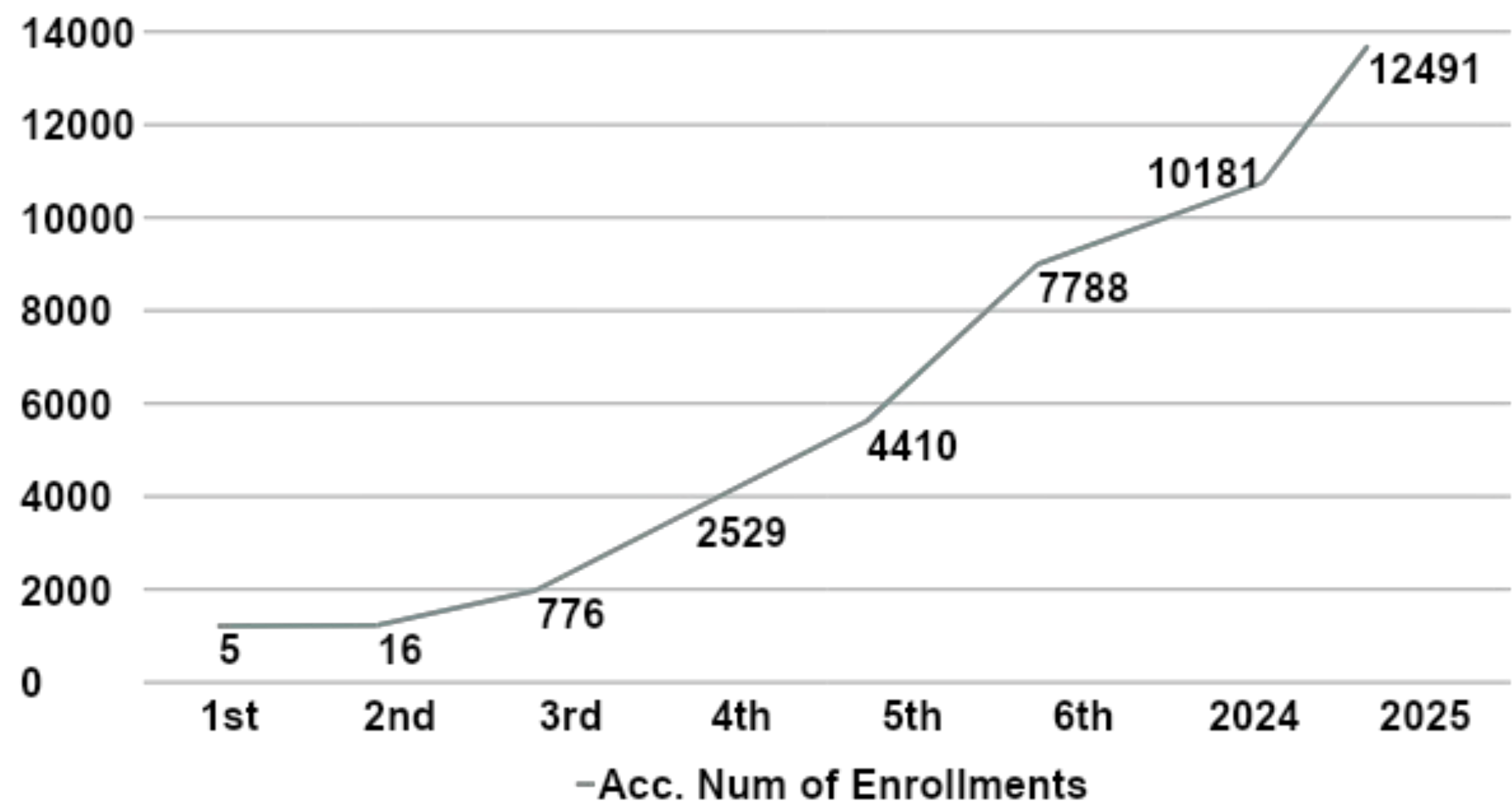
Report Accepted by RISC-V Global Forum 2020

NutShell: A Linux-Compatible RISC-V Processor Designed by Undergraduates



2. Current Teaching and Organization Model

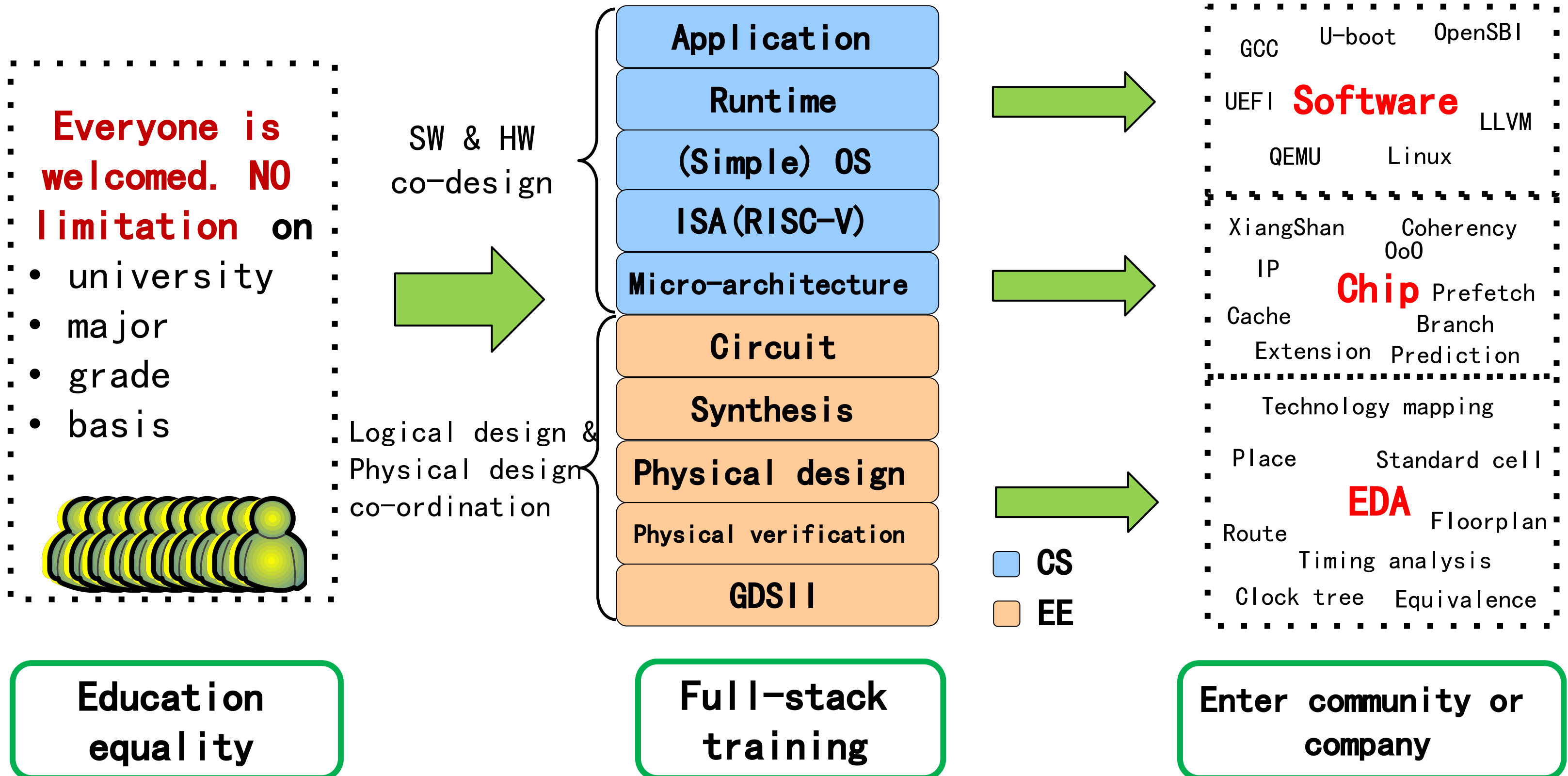
Explore Large-Scale (from 2021-)



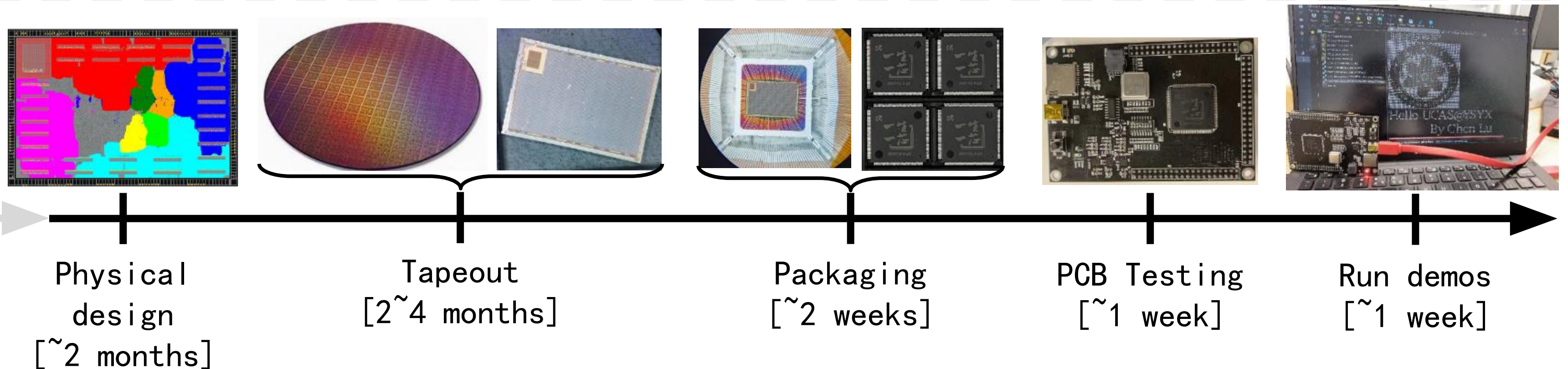
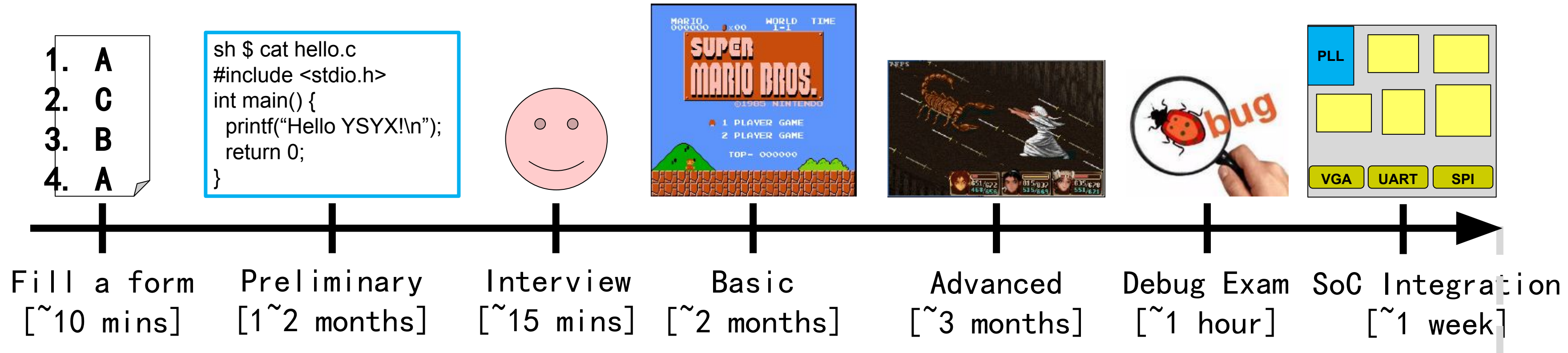
	1st	2nd	3rd	4th	5th	6th	2024	2025
Acc. Enrolls	5	16	776	2529	4410	7788	10181	12491

OSOC Course Design

Based on open-sourced, practice-oriented, open learning



Learning Roadmap



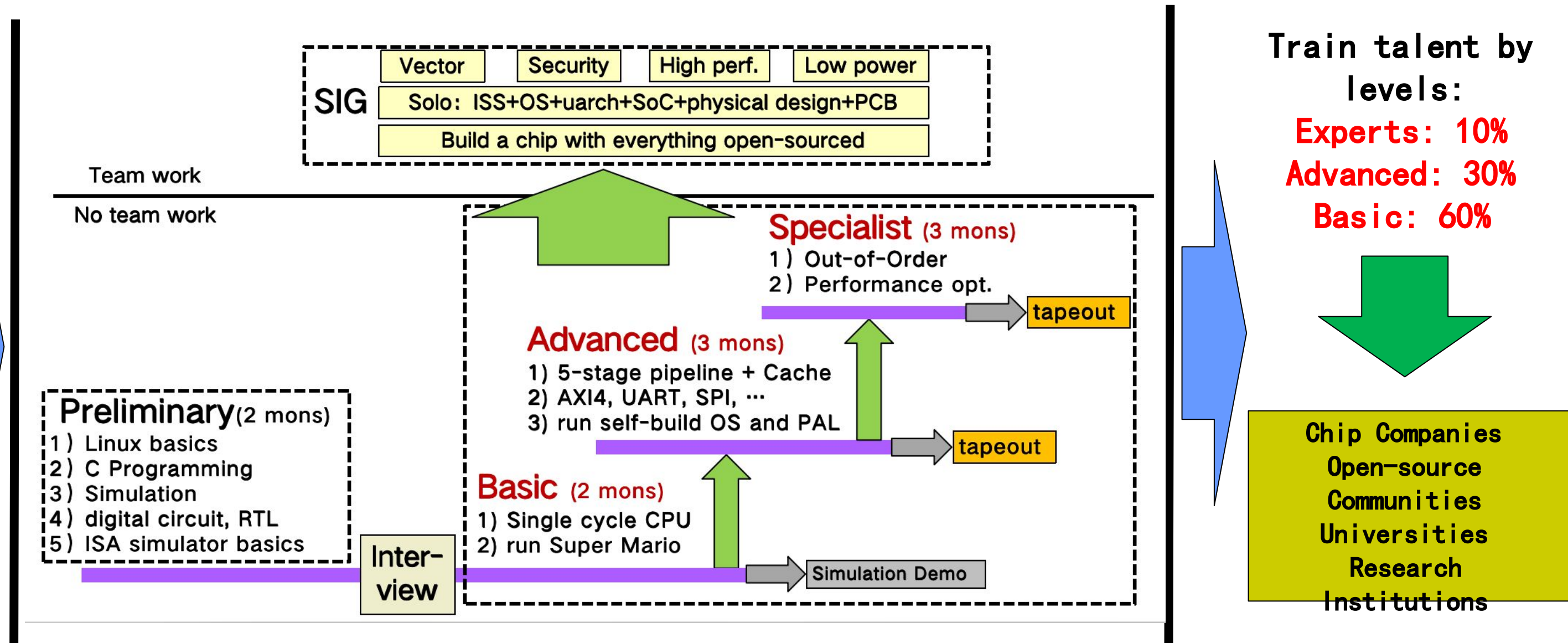
OSOC Organization Method

- **Teaching Assistant Team** : Train high-quality offline TAs (advanced level), combined with online TAs (basic or advanced level)
- Let students guide other students(**peer tutoring**) : advanced level TAs participate in SIG projects while also mentoring 'beginner' and 'intermediate' students

Recruit a large number of students (2000 - 4000), with a strict assessment process for registration (admitting 25%), while ensuring the proportions:

TA : Stu =

Students from the universities



Learning Materials are opened

The 6th "One Student One Chip" Program Home Page

- Time: Every Saturday 15:00~17:00 China Standard Time
 - Bilibili Live  | recording 

Learning Objectives

"One Student One Chip" will develop your general skills. At the end of the course, you will have a better understanding of the following questions:

- how processors are designed?
- how programs run on computers?
- how to optimize the performance of a processor?
- how to use/design the right tools for efficient debugging?
- how to write your own test cases for unit testing?
- how does an RTL design generate a flowable layout?

We will guide you to design a RISC-V pipeline processor. Run an operating system on your processor. Run a real game on the OS. The processor that achieves the target will be connected to the SoC and will be given the opportunity to tapeout.



- Course Website
- Handouts (260, 000 words)
- Slides (>800 pages, 85, 000 words)
- Videos (> 40 hours)

Linux system installation and basic usage

🔧 Install a Linux operating system

We're going to reuse the contents of the PA handout, and we're going to ask you to follow PA0 to install Linux OS.

🔧 Get "One Student One Chip" code framework

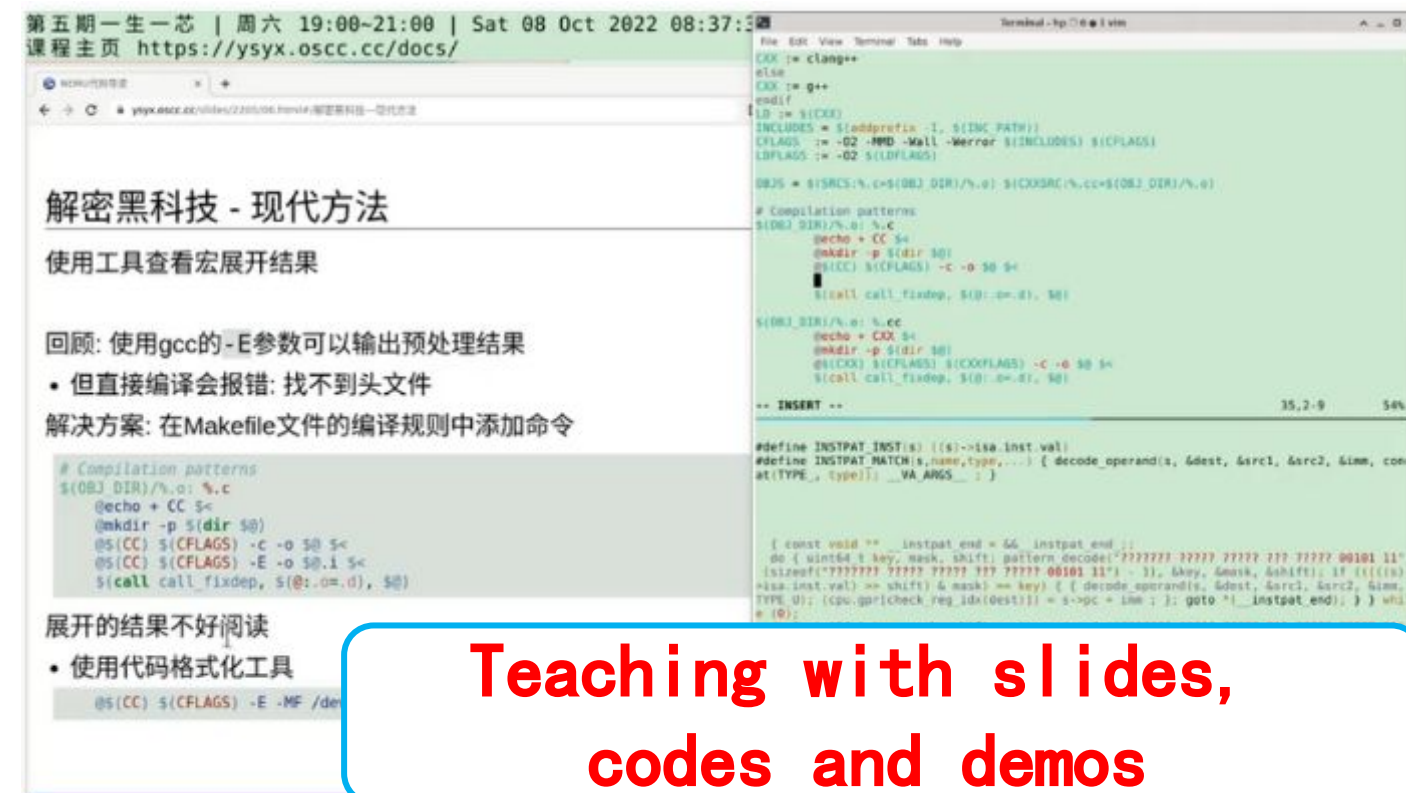
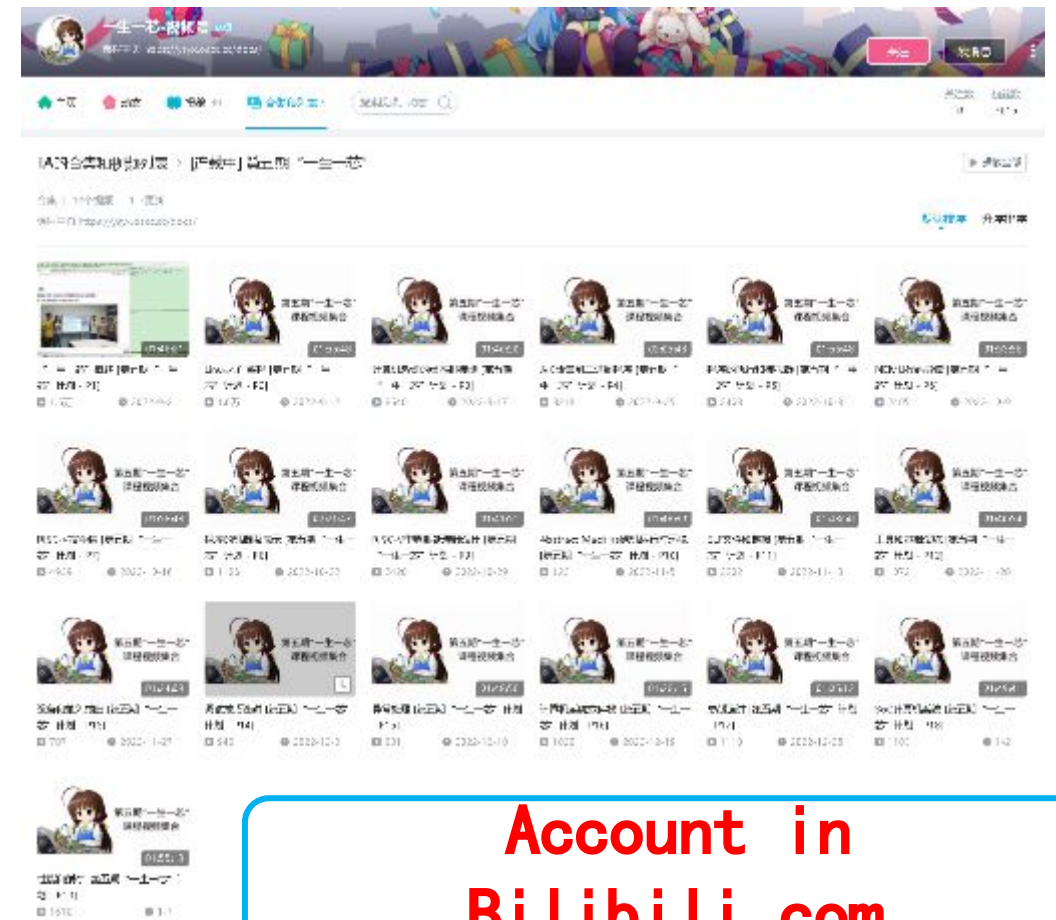
When you read the PA0 handout and proceed to the section on getting the PA framework code, you will be prompted with a box asking you to return to the content of the handout here.

First of all, please add a ssh key on github, please STFW on how to do that. Then get the framework code of "One Student One Chip" by the following command:

```
1 git clone -b master git@github.com:OSCPU/ysyx-workbench.git
```

Once you have it, you can go back to the appropriate place in the PA handout and continue reading. But you should also note that:

- Please use `ysyx-workbench` as the project directory in the PA handout, i.e. replace occurrence of `ics2022` in the PA handout with `ysyx-workbench`.
- When change the student number and name in `ysyx-workbench/Makefile`, you can leave the student number unchanged until you have completed the preliminary.



Handouts in English Version are available

The 6th 🇨🇳 🇺🇸 Study Handouts

Course Home ▾ Study Handouts ▾ Other Materials ▾ Select Languages ▾ ⚙

Learning Objectives

Learning Resource

Past Courses Home

Other resources

Record of events

The 6th "One Student One Chip" Program Home Page

- Time: Every Saturday 15:00~17:00 China Standard Time
 - [Bilibili Live](#) | [recording](#)

Learning Objectives

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We will guide you to design a RISC-V pipeline processor. Run an operating system on your processor. Run a real game on the OS. The processor that achieves the target will be connected to the SoC and will be given the opportunity to tapeout.

Learning Resource

- Icons can be clicked to jump to the appropriate resource
- Complete handouts can be viewed via the navigation bar at the top right of the page
- The content of the Stage S handout is still available

C = C language (program/simulator/system software) | **R** = RISC-V instruction set | **P** = processor design | **T** = tools

Stage	ID	Task	Handouts	Slides	Recording	C	R	P	T
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The 6th 🇨🇳 🇺🇸 Study Handouts

Course Home ▾ Study Handouts ▾ Other Materials ▾ Select Languages ▾ ⚙

Prestudy Stage

- Prestudy overview
- How to ask smart questions**
- Linux system installation and basic usage
- Reviewing the C language
- Build a verilog simulation environment
- Basic Digital Circuit Lab
- Complete PA1
- Submission of pre-study defense application

How to ask smart questions

[📄](#) **Fill in the general education questionnaire**

Before starting the first task of pre learning, please carefully read the content in sections "[Signup](#)" and "[FAQ](#)" on the official website and fill in "[The general education questionnaire of 'One Student One Chip'](#)". Note: The general education questionnaire can be repeated many times, and only those who score 100 can apply for admission defense.

[📄](#) **Read "How To Ask Questions The Smart Way" and "Stop Ask Questions The Stupid Ways", and write an essay of your thoughts on them**

Your first task in the prestudy is to read the articles "[How To Ask Questions The Smart Way](#)" and "[Stop Ask Questions The Stupid Ways](#)" and [Don't Ask Like a Retard](#), and write an 800-word essay about your experience of asking and being asked questions, and what you think about "good questioning" and "Independent problem solving through STFW and RTFM".

This task is not intended to be a waste of time, nor is it intended to prohibit you from asking any questions, but it is intended to show you "what is the right thing to do". When you are willing to work on these "right things" and try to ask questions in a professional way, you have already taken the first step to become a "professional".

[📄](#) **STFW, RTFM, RTFSC**

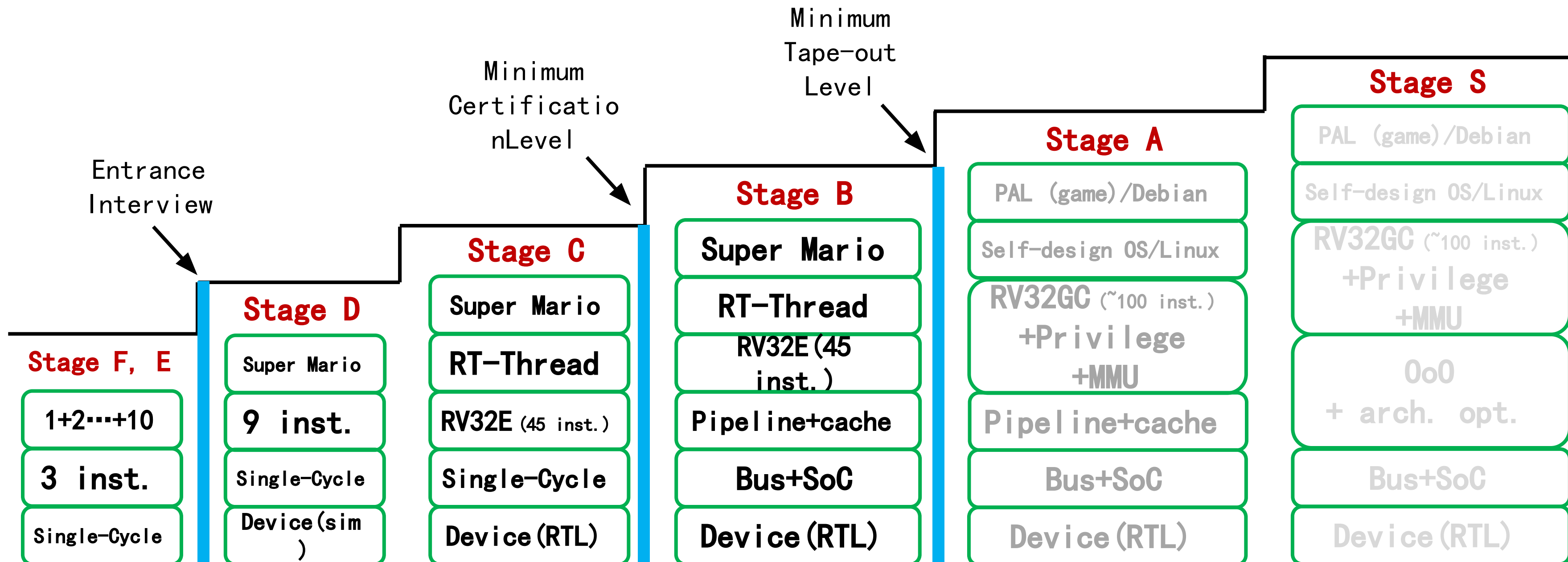
Try to find and understand the meanings of the three acronyms in the above article.

You may feel offended by the F word, but in fact the meaning of the F word is never the point, it just reflects the legend behind the three acronyms and makes them easier to remember. For example, RTFSC originated with the first words of Linus Torvalds, the father of Linux, in a reply to an email dated April 1, 1991, which is still available on the Internet mailing list. Interestingly,

BREAKING: New handouts will be released this month (ysyx.org/en), featuring a more beginner-friendly design.

Learning Stage Division (New handouts)

- Small, simple system → Large, complex system
- Small program → Real program



Learning Notes of a student

Time
dedicated

Date

Task

Issues
encountered

How to solve

	日期	计划任务	总时长	任务完成情况	卡了一段时间的bug																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																											
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Students' learning notes and meeting attendance

学号	姓名	学校	专业	年级	进度记录链接	"提问的智慧"读后感	实验报告	是否两周末更新进度记录	3.2	3.2 7	4 3	4.1 0	4.24	5.1	5.8	5.15	5.22	5.29	6.5	6.19	7.3	7.10	7.17	7.24	8.7	8.14
ysyx_22040020	毛英畅	天津大学	科学与工程; 辅修: 计算机	大四	ysyx_220020-毛英畅-天津大学-学习记录	ysyx_220020-毛英畅-天津大学-读后感		两周末更新	3.20			2022.4.11	S-关键: PA1	2022.202	npc-c	202	2022.2022	7.10	请假					2022.8.7	请假	
ysyx_22040047	吴浩宇	东北大学	计算机科学与技术	大二	ysyx_220047-吴浩宇-东北大学-学习记录	ysyx_220047-吴浩宇-东北大学-读后感			2022.3.20		2022.4.10	请假	PA2-3	npc读	2022.2022	6.1	2022	2022.7.17	请假							
ysyx_22040091	冯浩原	中国科学院大学	计算机科学与技术	大三	ysyx_220091-冯浩原-中国科学院大学-学习记录	ysyx_220091-冯浩原-读后感	ysyx_220091-冯浩原-预学习实验报告		2022.3.20			2022.4.24	清	PA4.1												
ysyx_22040030	刘朋丰	东北大学秦皇岛分校	计算机类	大一	ysyx_220030-刘朋丰-东北大学秦皇岛分校-学习记录	ysyx_220030-刘朋丰-读后感	ysyx_220030-刘朋丰-实验报告		2022.3.20	2022.3	2022.4.10	请假	PA2													
ysyx_22040063	包子旭	河南理工大学	计算机科学与技术	大二	ysyx_220063-包子旭-河南理工大学-学习记录	ysyx_220063-包子旭-读后感			2022.3.20			2022.4.24	清	PA2	2022.1	PA2	2022.2022	7.3	2022.7.17	请假			2022.8.7	请假	2022.8.14	请假
ysyx_22040031	苗恒	青岛科技大学	电子信息	研一	ysyx_220031-苗恒-青岛科技大学-学习记录	ysyx_220031-苗恒-读后感	ysyx220031 苗恒 实验报告		2022.3.20			PA2	PA2 1	PA2	PA2	PA2	PA2	2-trace					单周期 SoC总	参加会议		
ysyx_22040012	毕睿	海南大学	电子信息工程	大二	副本-ysyx_220012-毕睿-海南大学-学习记录	ysyx_220012-毕睿-读后感	ysyx_220012-毕睿-实验报告.pdf		2022.3.20	2022.4	2022.4.24	清	PA2	1	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022
ysyx_22040099	蔡惠荣	太原理工大学	通信工程	大二	ysyx_220099-蔡惠荣-太原理工大学-学习记录	ysyx_220099-蔡惠荣-读后感	ysyx_220099-蔡惠荣-实验报告		2022.3.20					PA1	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022
ysyx_22040025	邱凡尧	东北大学	物联网工程	大二	ysyx_220025-邱凡尧-东北大学-学习记录	ysyx_220025-邱凡尧-读后感	ysyx_22040025-邱凡尧-实验报告		2022.3.20			npc-1	进行中	PA2-2	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022
ysyx_22040034	杜奕明	太原理工大学	软件工程	大四	ysyx_220034-杜奕明-太原理工大学-学习记录	ysyx_220034-杜奕明-读后感	完成PA1, 无报告		2022.3.20			npc-1	进行中	PA2-1	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022
ysyx_22040094	黎梓浩	国防科技大学	软件工程	大二	ysyx_220094-黎梓浩-国防科技大学-学习记录	ysyx_220094-黎梓浩-读后感	完成至PA1.1, 无报告		2022.3.20	2022.3	2022.4.24	清	PA2	2-k	PA1	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022
ysyx_22040046	王凯	中国科学技术大学	计算机科学与技术	大三	ysyx_220046-王凯-中国科学技术大学-学习记录	ysyx_220046-王凯-读后感	ysyx_220046-王凯-实验报告		2022.3.20	2022.3	2022.4.24	清	PA2	2-k	PA1	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022
ysyx_22040073	关常润	华南理工大学	集成电路工程	研一	ysyx_22040073-关常润-学习记录	ysyx_22040073-关常润-读后感	完成至PA1.1		2022.3.20	2022.4	2022.4.24	清	PA1	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022
ysyx_22040096	叶创豪	杭州电子科技大学	软件工程	大二	ysyx_220096-叶创豪-杭州电子科技大学-学习记录	ysyx_220096-叶创豪-读后感	ysyx_220096-叶创豪-实验报告		2022.3.20	2022.4	2022.4.24	清	PA2	1	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022
ysyx_22040080	孙佳丰	电信科学技术研究院	电子科学与技术	研三	ysyx_220080-孙佳丰-电信科学技术研究院-学习记录	ysyx_220080-孙佳丰-读后感	完成至PA1.1	一周未更新	3.20			2022.4	2022.4.24	清	PA2	2	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022
ysyx_22040040	祝静	天津理工大学	集成电路工程	研一	ysyx_220040-祝静-天津理工大学-学习记录	ysyx_220040-祝静-读后感	ysyx_220040-祝静-实验报告		2022.3.20			PA2	1	完成	PA1	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022
ysyx_22040070	杨利民	北京工商大学	软件工程	大二	ysyx_220070-杨利民-北京工商大学-学习记录	ysyx_220070-杨利民-读后感	ysyx_220070-杨利民-实验报告	等待更新中	3.20			npc-1	完成	PA1	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022
ysyx_22040163	王墨宇	南通大学	计算机科学与技术	大二	ysyx_22040163-王墨宇-南通大学-学习记录	ysyx_22040163-王墨宇-读后感	ysyx_22040163-王墨宇-实验报告		2022.3.20			PA3	3	PA3	3	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022
ysyx_22040068	王俊	海南大学	保研至微电子学, 研究方向:	大四	ysyx_220068-王俊-学习记录	ysyx_220068-王俊-读后感	截至PA1.1 (问题有点多, 还没来得及汇总和撰写实验报告)	请假5.31	2022.3.20	2022.3.20	2022.3.20	2022.3.20	2022.3.20	2022.3.20	2022.3.20	2022.3.20	2022.3.20	2022.3.20	2022.3.20	2022.3.20	2022.3.20	2022.3.20	2022.3.20	2022.3.20	2022.3.20	2022.3.20
ysyx_22040188	徐铭伟	西安电子科技大学	信息与通信工程	研一	ysyx_22040188-徐铭伟-西安电子科技大学-学习记录	ysyx_22040188-徐铭伟-读后感	完成至PA1.1	两周末更新	2022.3.20	2022.3.20	2022.3.20	2022.3.20	2022.3.20	2022.3.20	2022.3.20	2022.3.20	2022.3.20	2022.3.20	2022.3.20	2022.3.20	2022.3.20	2022.3.20	2022.3.20	2022.3.20	2022.3.20	2022.3.20
ysyx_22040214	朱吉宏	哈尔滨工业大学	电子信息	研一	ysyx_22040214-朱吉宏-哈尔滨工业大学-学习记录	ysyx_22040214-朱吉宏-读后感	ysyx_22040214-朱吉宏-实验报告		2022.3.20			npc-1	完成	PA1	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022
ysyx_22040539	周有丰	清华大学	电子科学与技术	大四	ysyx_22040539-周有丰-清华大学-学习记录	ysyx_22040539-周有丰-读后感	ysyx_22040539-周有丰-实验报告	两周末更新	2022.3.20	2022.3.20	2022.3.20	2022.3.20	2022.3.20	2022.3.20	2022.3.20	2022.3.20	2022.3.20	2022.3.20	2022.3.20	2022.3.20	2022.3.20	2022.3.20	2022.3.20	2022.3.20	2022.3.20	2022.3.20
ysyx_22040017	解博元	东北大学秦皇岛分校	计算机科学与技术	大二	ysyx_220017-解博元-东北大学秦皇岛分校-学习记录	ysyx_220017-解博元-读后感		请假5.31	2022.3.20	2022.3.20	2022.3.20	2022.3.20	2022.3.20	2022.3.20	2022.3.20	2022.3.20	2022.3.20	2022.3.20	2022.3.20	2022.3.20	2022.3.20	2022.3.20	2022.3.20	2022.3.20	2022.3.20	2022.3.20
ysyx_22040067	李珍琪	国防科技大学	计算机科学与技术	大三	ysyx_220067-李珍琪-国防科技大学-学习记录	ysyx_220067-李珍琪-读后感	ysyx_220067-李珍琪-实验报告	两周末更新	2022.3.20	2022.3.20	2022.3.20	2022.3.20	2022.3.20	2022.3.20	2022.3.20	2022.3.20	2022.3.20	2022.3.20	2022.3.20	2022.3.20	2022.3.20	2022.3.20	2022.3.20	2022.3.20	2022.3.20	2022.3.20
ysyx_22040001	蒋雨彤	深圳大学	计算机科学与技术	大四	ysyx_220001-蒋雨彤-深圳大学-学习记录	ysyx_220001-蒋雨彤-读后感	ysyx_220001-蒋雨彤-实验报告	两周末更新	2022.3.20	2022.3.20	2022.3.20	2022.3.20	2022.3.20	2022.3.20	2022.3.20	2022.3.20	2022.3.20	2022.3.20	2022.3.20	2022.3.20	2022.3.20	2022.3.20	2022.3.20	2022.3.20	2022.3.20	2022.3.20
ysyx_22040178	王九龙	北京邮电大学	电子科学与技术	大三	ysyx_22040178-王九龙-北京邮电大学-学习记录	ysyx_22040178-王九龙-读后感	ysyx_22040178-王九龙-实验报告	两周末更新	3.20	2022.3.27	2022.3.27	2022.3.27	2022.3.27	2022.3.27	2022.3.27	2022.3.27	2022.3.27	2022.3.27	2022.3.27	2022.3.27	2022.3.27	2022.3.27	2022.3.27	2022.3.27	2022.3.27	2022.3.27
ysyx_22040374	崔家贺	南开大学	软件工程	大二	ysyx_22040374-崔家贺-学习记录	ysyx_22040374-崔家贺-读后感	ysyx_22040374-崔家贺-实验报告		2022.3.20	2022.3	2022.4.24	清	PA2	3	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022
ysyx_22040154	徐步青	东南大学	电子科学与技术	大四	ysyx_22040154-徐步青-东南大学-学习记录	ysyx_22040154-徐步青-读后感	ysyx_22040154-徐步青-实验报告		2022.3.20			PA2	3	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022
ysyx_22040193	英文强	中国科学技术大学	电子信息	研二	ysyx_22040193-英文强-中国科学技术大学-学习记录	ysyx_22040193-英文强-读后感	ysyx_22040193-英文强-实验报告		2022.3.20			PA2	2	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022
ysyx_22040142	刘森	上海海洋大学	计算机科学与技术	大三	ysyx_22040142-刘森-上海海洋大学-学习记录	ysyx_22040142-刘森-读后感	ysyx_22040142-刘森-实验报告		2022.3.20			PA2	2	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022
ysyx_22040200	乌鑫龙	北京师范大学珠海分校	计算机科学与技术	大三	ysyx_22040200-乌鑫龙-北京师范大学珠海分校-学习记录	ysyx_22040200-乌鑫龙-读后感	ysyx_22040200-实验报告	请假5.31	3.20			npc-1	完成	PA2	2	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022
ysyx_22040414	林沛润	广东工业大学	集成电路设计与集成系统	大三	ysyx_22040414-林沛润-广东工业大学-学习记录	ysyx_22040414-林沛润-读后感	ysyx_22040414-林沛润-实验报告		2022.3.20	2022.3.27	2022.3.27	2022.3.27	2022.3.27	2022.3.27	2022.3.27	2022.3.27	2022.3.27	2022.3.27	2022.3.27	2022.3.27	2022.3.27	2022.3.27	2022.3.27	2022.3.27	2022.3.27	2022.3.27
ysyx_22040413	晏凯	电子科技大学	电子信息工程	研二	ysyx_22040413-晏凯-电子科技大学-学习记录	ysyx_22040413-晏凯-读后感	ysyx_22040413-晏凯-实验报告		2022.3.20	2022.4	2022.4.24	清	PA2	2	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022
ysyx_22040595	郑佳纯	华南理工大学	电子科学与技术	大四	ysyx_22040595-郑佳纯-华南理工大学-学习记录	ysyx_22040595-郑佳纯-读后感	ysyx_22040595-郑佳纯-实验报告		2022.3.20			PA2	2	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022	2022.2022
ysyx_22040301	于皓哲	沈阳工业大学	电子科学与技术	研二	ysyx_22040301-于皓哲-沈阳工业大学-学习记录	ysyx_22040301-于皓哲-读后感	ysyx_22040301-于皓哲-实验报告	请假5.31	3.20	2022.4	2022.4	2022.4	2022.4	2022.4	2022.4	2022.4	2022.4	2022.4	2022.4	2022.4	2022.4	2022.4	2022.4	2022.4	2022.4	2022.4
ysyx_22040562	李张勋	华中科技大学	集成电路设计与集成系统	大三	ysyx_22040562-李张勋-华中科技大学-学习记录	ysyx_22040562-李张勋-读后感	ysyx_22040562-李张勋-实验报告		2022.3.20			PA2														

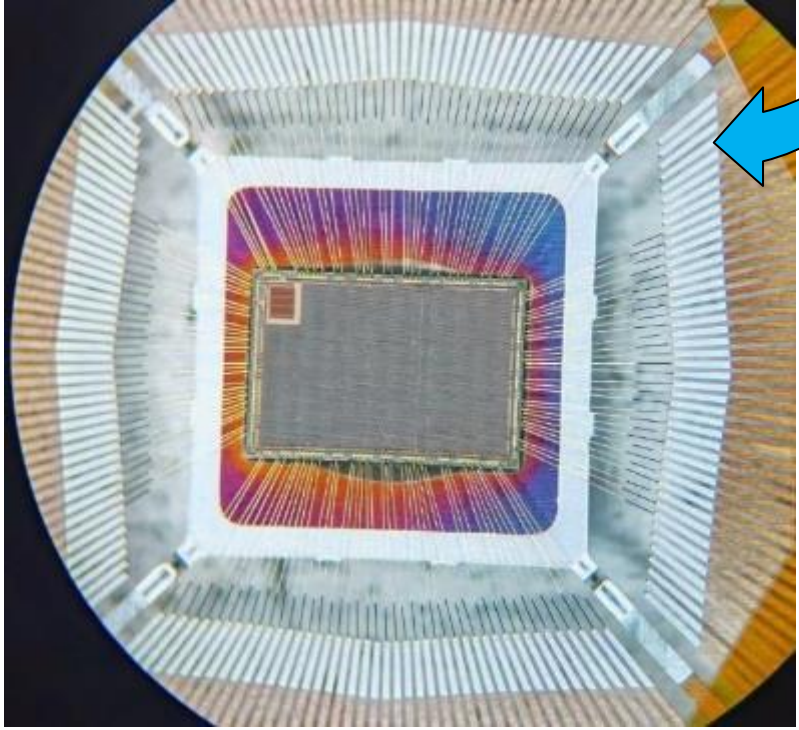
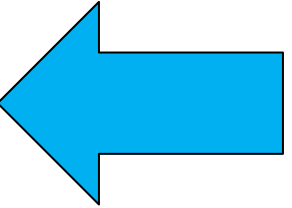
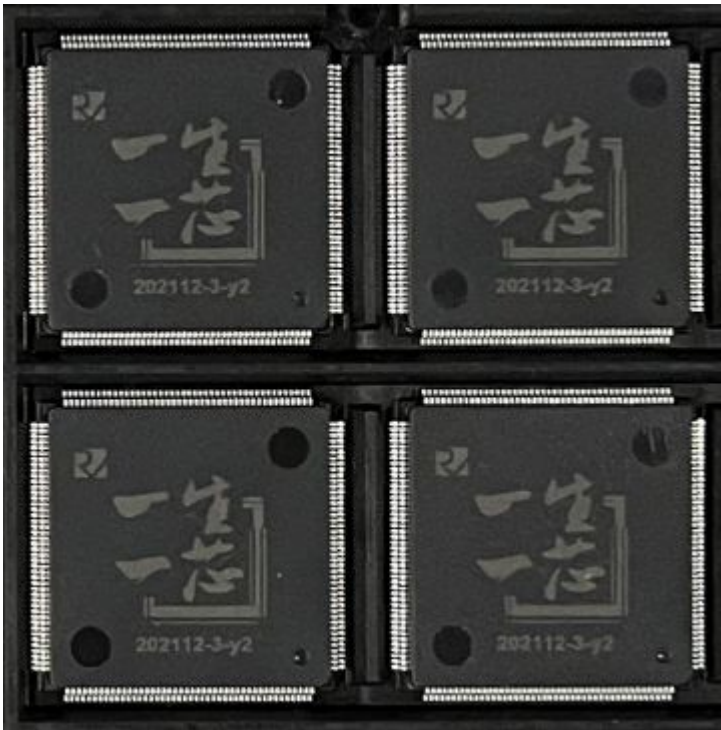
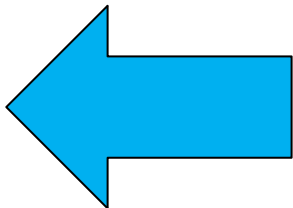
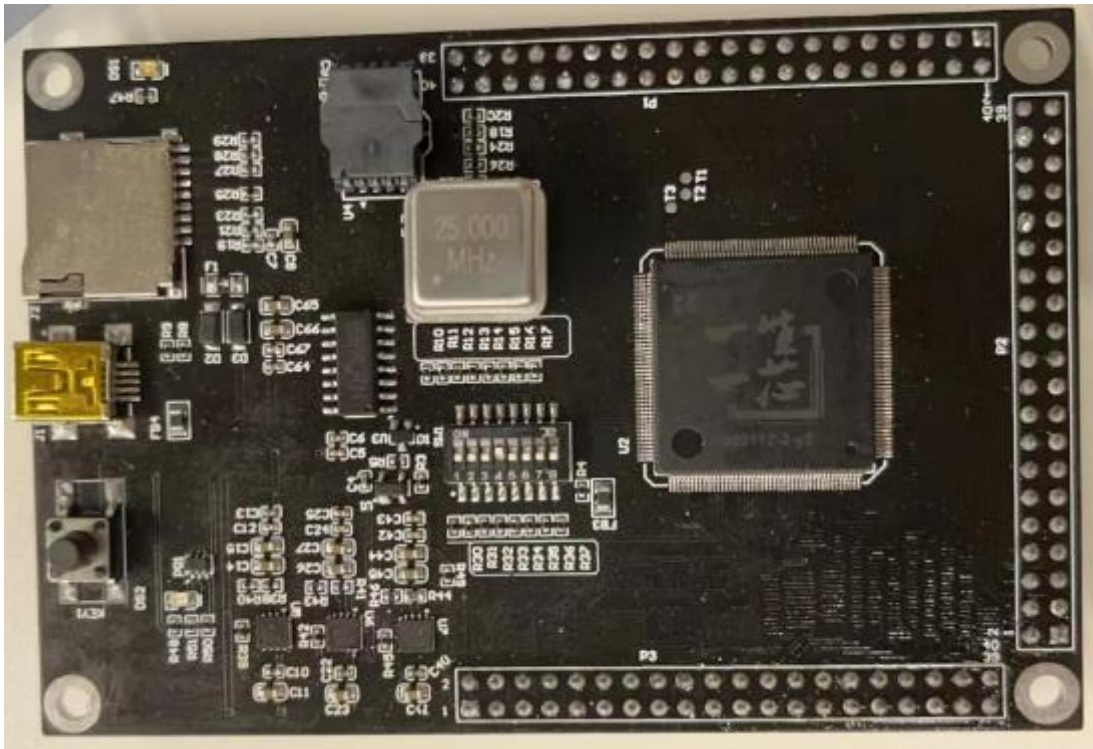
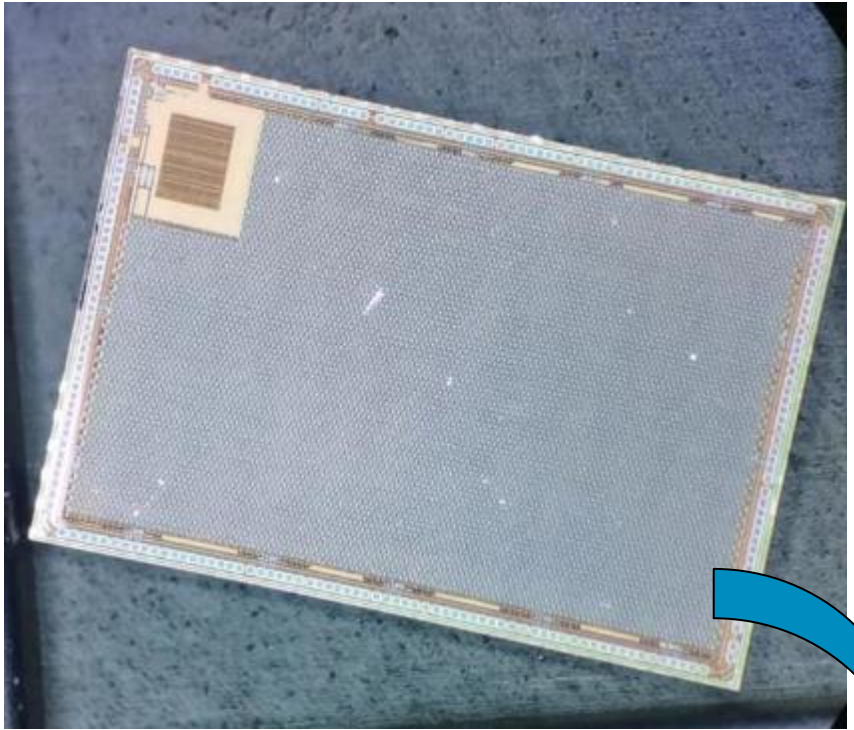
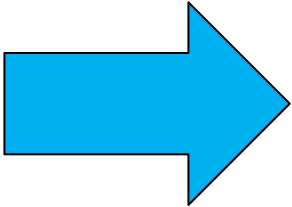
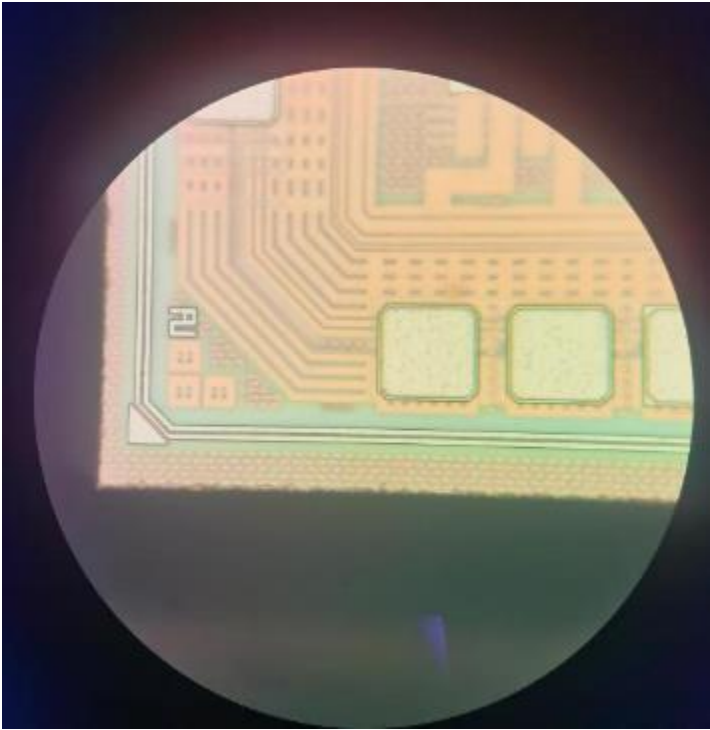
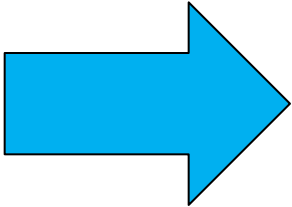
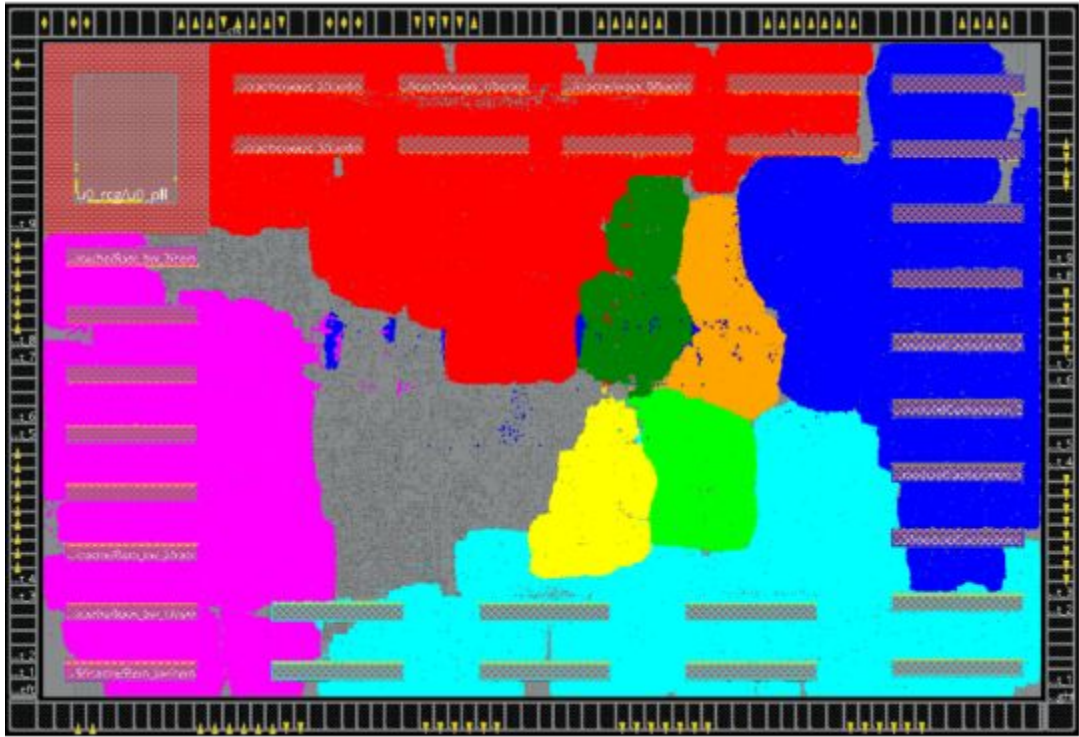
No Deadline for Learning

- The time spent by students to finish learning varies (from weeks to years)
 - Different universities, different majors, different grades, different basics
 - Some of them learn more quickly than others
 - Some of them start earlier than others
 - Some of them are busier than others with their own courses
- Students without any basics may spend > 500 hours
 - 500h: the time to take compulsory courses and finish all assignments
- Students can always learn with her/his own timing schedule
 - Once she/he finishes, she/he can apply for interview/exam

Online Debug Exam, instead of paper exam

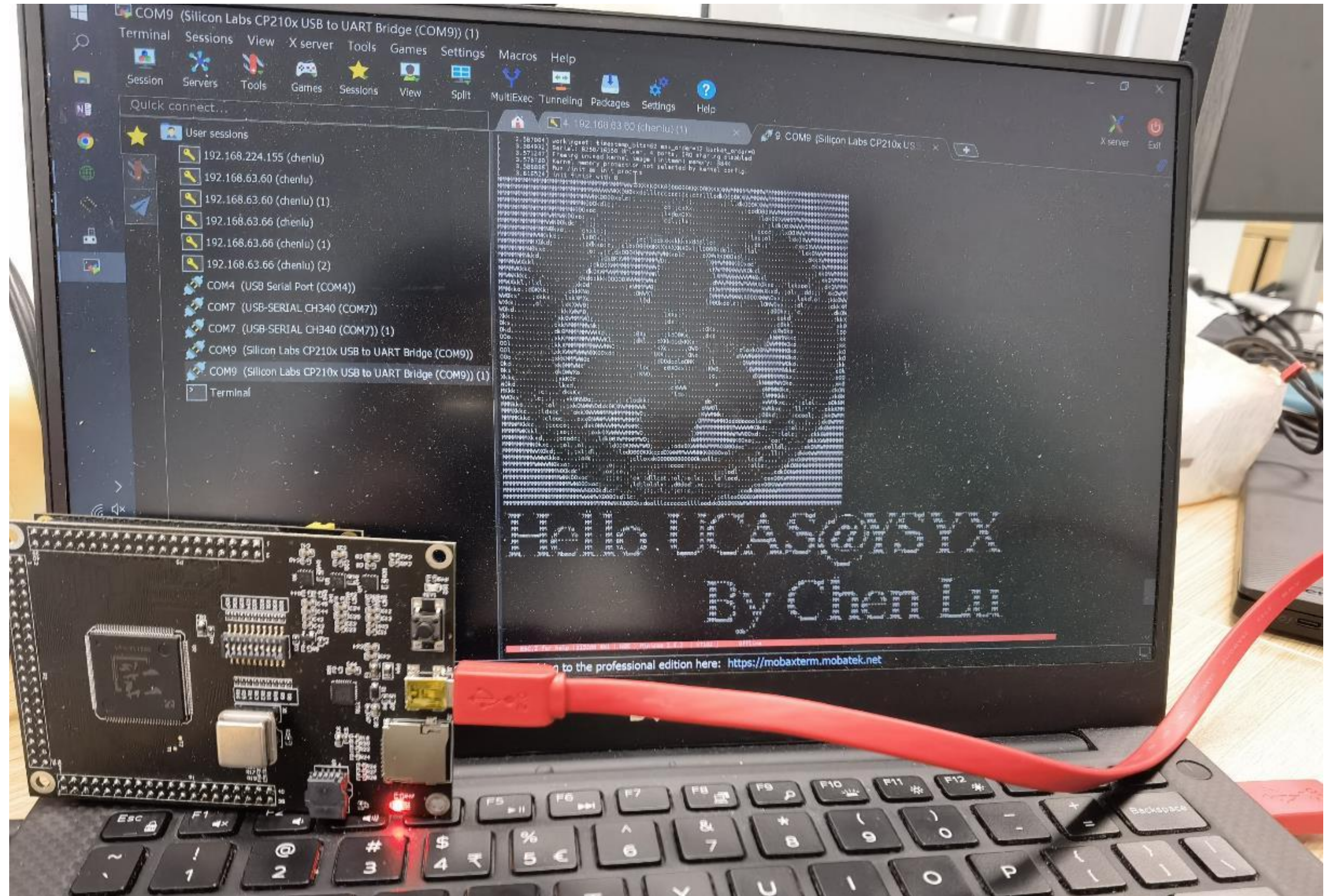
- When students apply for tape-out, TA will inject some bugs randomly in students' project
 - Including hardware, software, building and simulation system bugs
- Required to debug within 1 hour in an online meeting
 - share screen throughout the entire process
- To evaluate whether
 - student knows enough details in the whole project
 - student can analyze problem from the respect of sw-hw co-operation
 - student knows when to use the right tools during debugging
 - student can solve new problems by herself/himself

Chip & Board

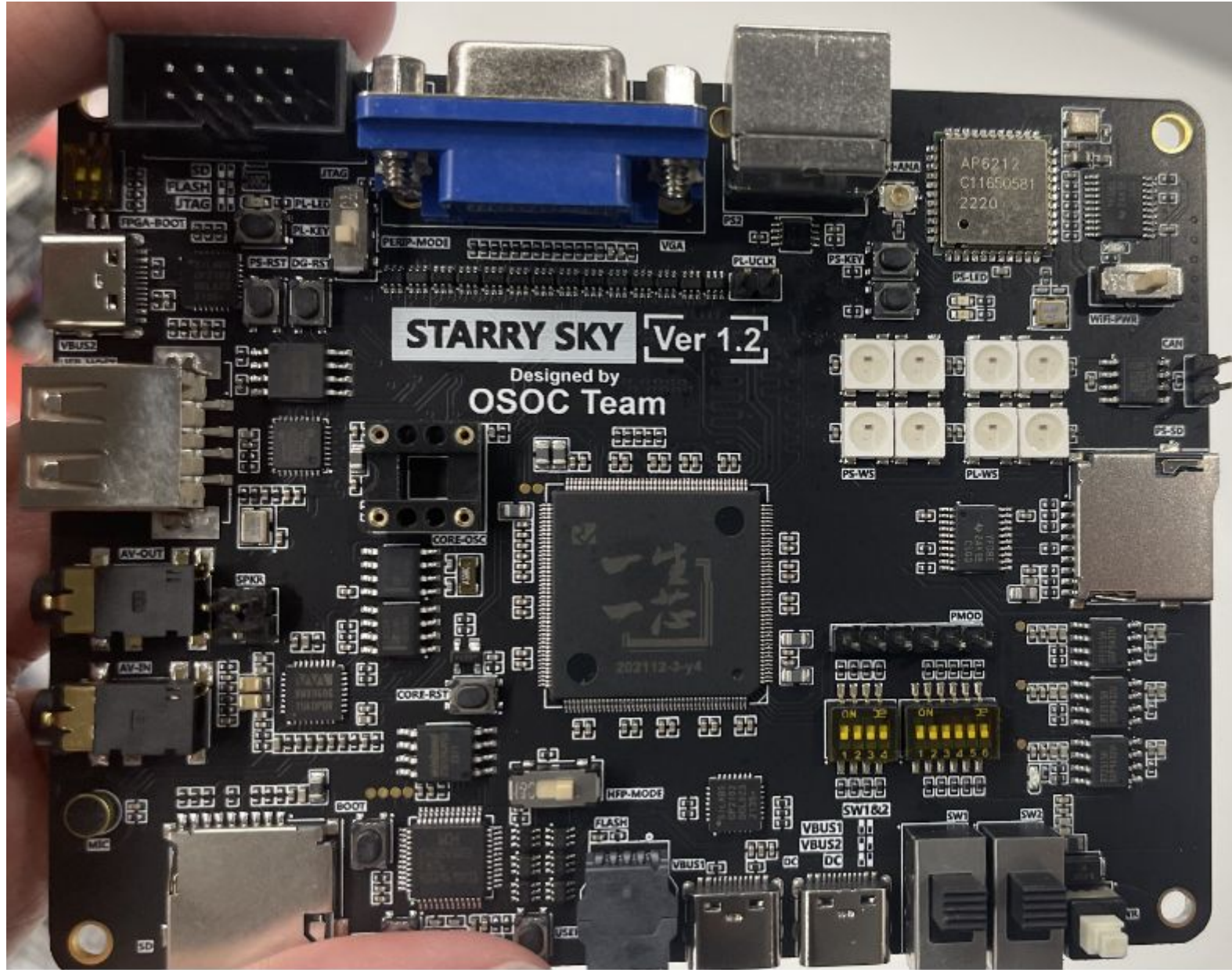


Demo by students

- A computer science student who began studying OS0C as a junior
- Load Linux from flash and boot successfully, showing the CAS logo



Delivering PCB to students

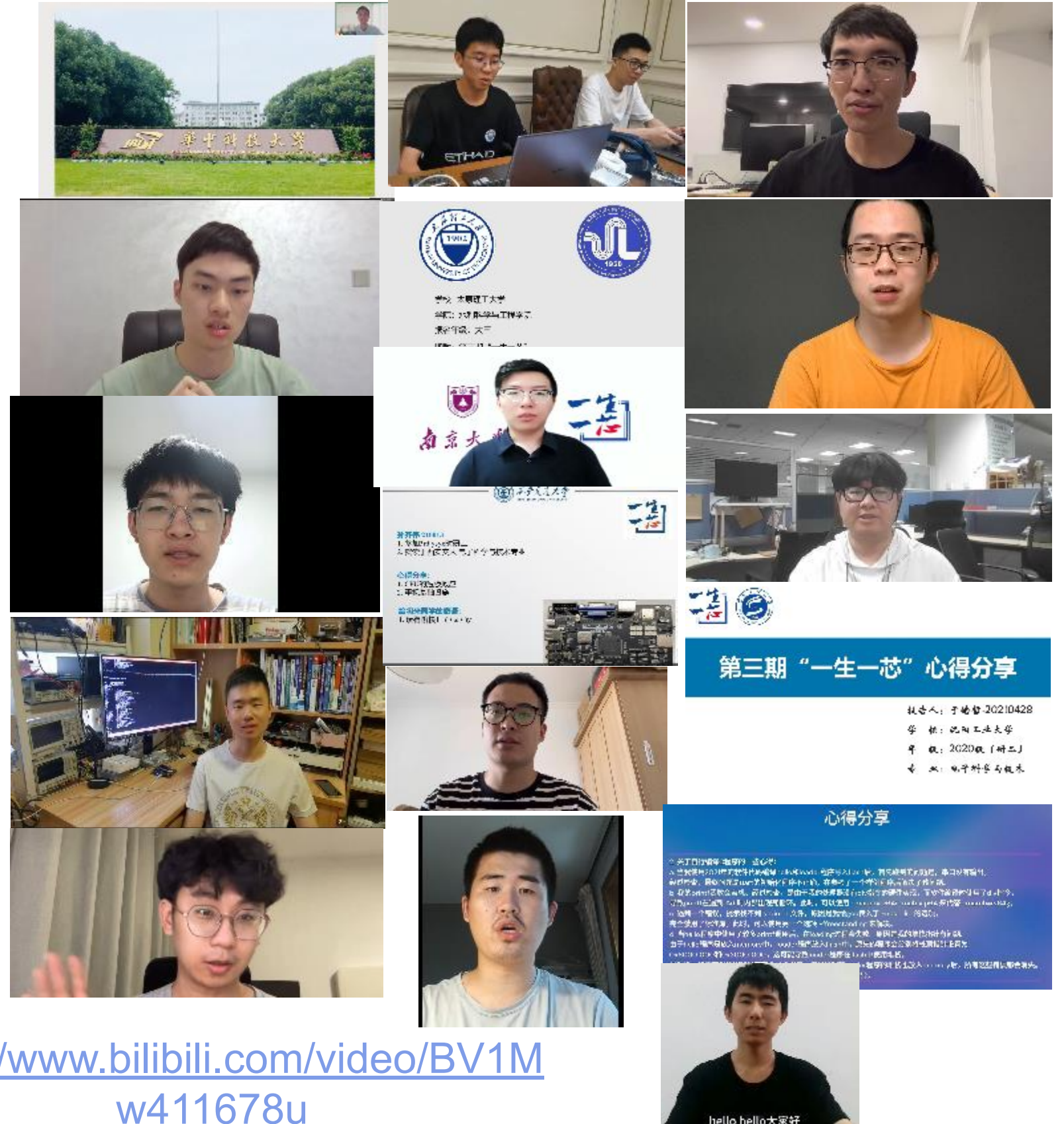
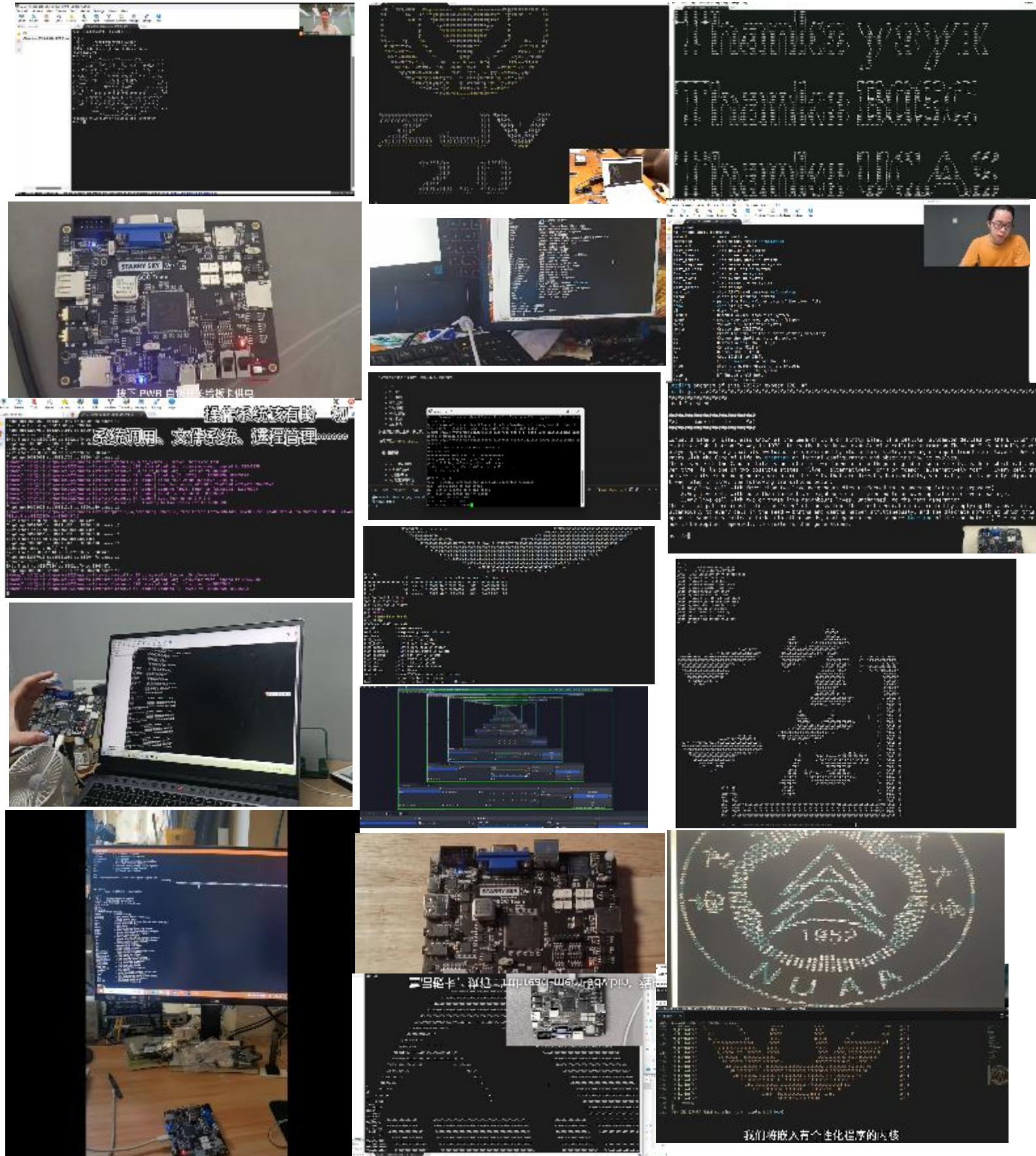


PCB designed by OSOC



Before delivering

Brought up Chips, Ran OS & Applications



<https://www.bilibili.com/video/BV1Mw411678u>

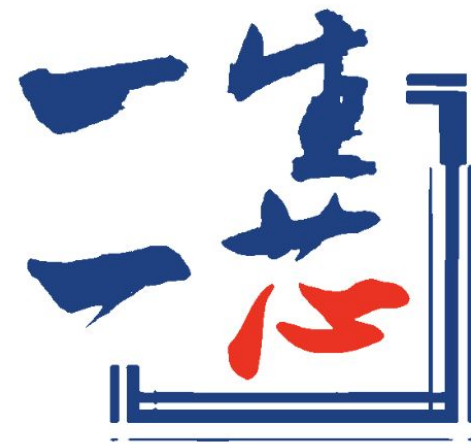
Enroll Anytime, Open Year-Round



Website
ysyx.org/en



Telegram
Group

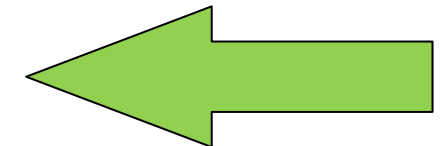


Start From Scratch
Create Your Own
RISC-V[®] Processor

Project Info

PDF Download

Signup



Scan the QR code or visit ysyx.org/en and click
"Signup"

3. Collaboration

OSOC Roadshow Event

- Our journey is ongoing, we warmly invite you to reach out and extend an invitation to OSOC to visit your location!



Professor in Kazakhstan introduces OSOC in his class

- Professor Nursultan Kabylkas, Nazarbayev University
 - Register an elective course in NU: Microprocessor Design and Verification 101 (CS335)
 - Train the first batch of RISC-V processor chip design talents for Kazakhstan

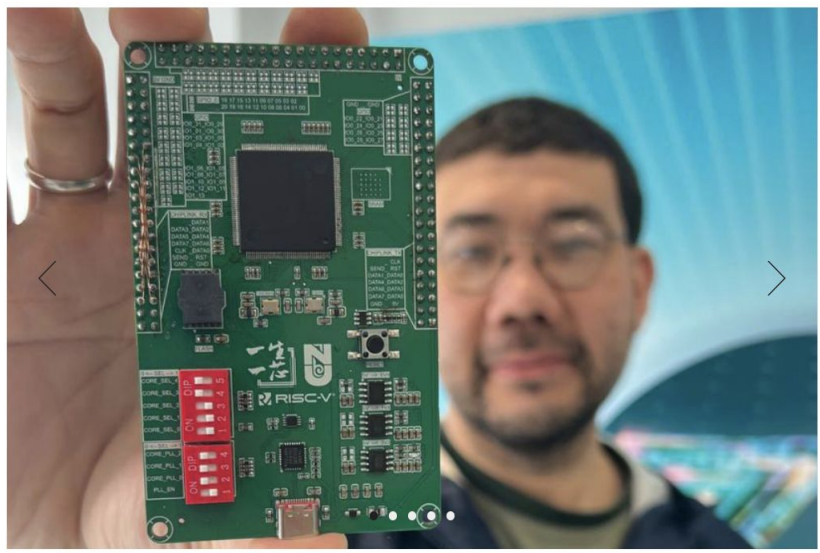


Kazakhstan Got its First Self-Designed Processor Chip from OSOC

- In March 2025, student Olzhas in Kazakhstan got his own designed RISC-V chip and tested successfully
- The chip is totally designed through OSOC and taped out by OSOC
- The first self-designed processor chip, demonstrating a big milestone in Kazakhstan

NU SEDS Researchers Successfully Fabricate Kazakhstan's First Locally Designed Microchip

11.03.2025



Kazakhstan has taken a groundbreaking step in technological innovation with the successful fabrication of its first locally designed microchip, marking a significant milestone for the nation's semiconductor industry.

Developed by researchers from Nazarbayev University's School of Engineering and Digital Sciences (NU SEDS), Department of Computer Science, the microchip was produced through an international collaboration with the University of Chinese Academy of Sciences and the Beijing Institute of Open Source Chip, as part of the "One Student, One Chip" program. The project also received critical support from local startup TEXER.AI, which was backed by a QazInnovation grant, reinforcing



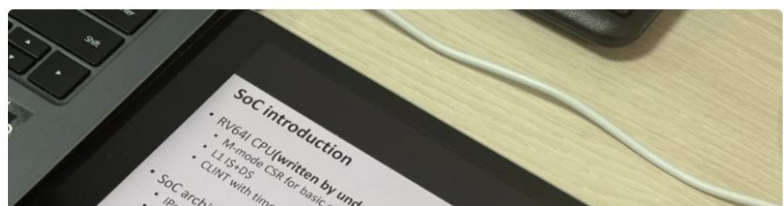
Made in Kazakhstan: a new stage in the development of the semiconductor industry

24 May, 18:45 20977



Future of Kazakhstan's Semiconductor Industry Discussed Experts

On May 23, 2025, Nazarbayev University (NU) hosted the forum "Charting the Silicon Road: Digital Hardware Design Development and Education for Modern Kazakhstan", [DKnews.kz](#) reports.



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Azul Linhas Aéreas

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O céu do São João é mais Azul. Visite Site

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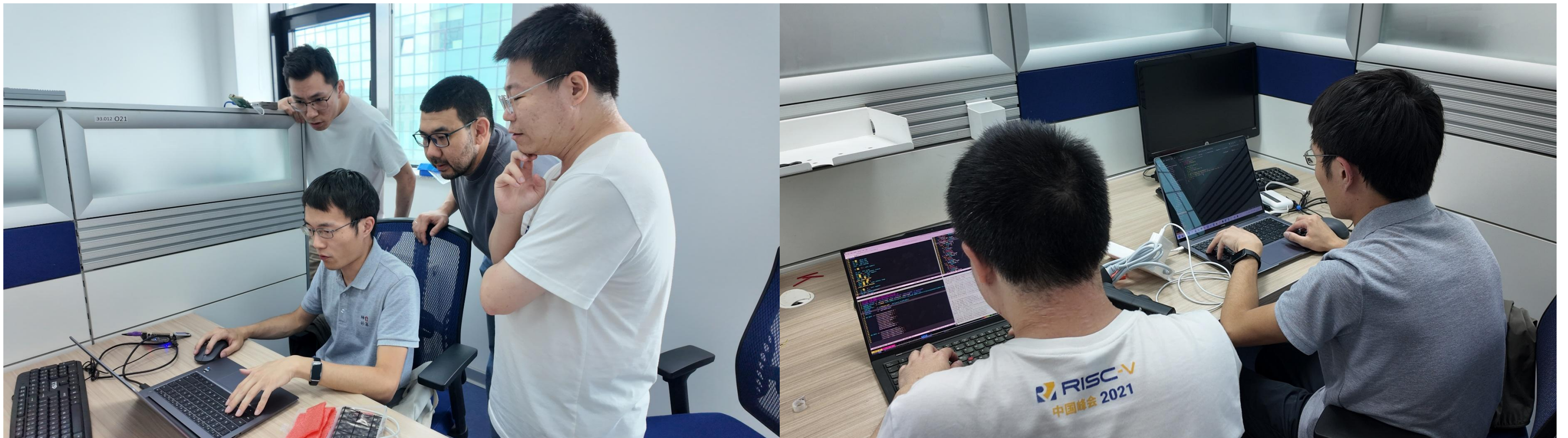
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24 June, 14:07 8932

OSOC Base in Kazakhstan Nazarbayev University

- Professor Nursultan Kabylkas runs a lab, and most of the students there have joined the OSOC program
- Now it becomes the base and the workshop for OSOC students at NU
- Forming an active OSOC student community



Professor in Japan adopts the OSOC program

- Professor Nobuaki Kobayashi, Nihon University
 - Train students' RISC-V design skills and explore RISC-V-related research topics
 - Willing to organize students to translate the OSOC handouts into Japanese to attract more Japanese students to study

发件人: Nobuaki Kobayashi <kobayashi.nobuaki@nihon-u.ac.jp>
发送时间: 2024年3月29日 19:20
收件人: ysyx@bosc.ac.cn
主题: 关于 "一生一芯" 项目, 日本大学

您好。

我叫小林, 来自日本大学科学技术学院。我对你们的 "一生一芯" 项目非常感兴趣。

我的实验室最近开始研究 RISC-V。

我相信这个项目不仅能促进我们学生的发展, 还能带来各种研究项目。

我的实验室里有几个中国学生, 他们希望参与这个项目。

如果您能允许他们参与该项目, 我将不胜感激。

如果您能积极考虑我的建议, 我将不胜感激。

如果需要任何费用, 我很乐意支付课程费用。非常感谢您的合作。

附注: 请注意, 本文是使用翻译工具编写的。如果我们不能这样做, 请原谅我们。

——原始邮件——

发件人: "Nobuaki Kobayashi" <kobayashi.nobuaki@nihon-u.ac.jp>
发送时间: 2024-04-15 10:31:18 (星期一)
收件人: "Yungang Bao" <baoyg@ict.ac.cn>
抄送: "Biwei Xie" <xiebiwei@ict.ac.cn>, ysyx@bosc.ac.cn, yuzihao <yuzihao@ict.ac.cn>, miaoyuyang@ict.ac.cn
主题: Re: Re: Re: Re: 关于 "一生一芯" 项目, 日本大学

Dear Prof. Yungang Bao,

Thank you very much for your guidance.

I think this is a very progressive initiative that provides equal opportunities to students from all over the world and rewards the efforts of passionate and motivated students.
To give you some background on my department, in recent years, Japan's declining birthrate has become an increasingly serious problem, and it is difficult to make ends meet (in terms of the business of education, since we are a private university) if we have only Japanese students. Therefore, we are actively accepting students from overseas, and about 40% of this year's new students of my department are international students. Of these, students from China account for more than 95%.

My main research areas are biological signal processing and digital circuits, and so RISC-V is a very suitable theme for me, but it is difficult for me to promote a comprehensive education because I am the only one teacher in my laboratory.
With this background, it is very attractive for me to participate in the efforts you are promoting, and I think it will be very beneficial for the students as well.

We may be able to assist in the near future with translating the materials into Japanese.
In any case, we are very grateful since you provide us with English-language materials, as I believe that Japanese students will be able to take the lectures well enough with these materials.

Thank you for your continued support.

Best regards,

小林伸彰
日本大学理工学部精密機械工学科
〒274-8501 千葉県船橋市習志野台7丁目24番1号 6号館2階623室

OSOC University Collaboration Pathway

Initial Stage

Strengthened Stage

In-Depth Stage

Plan A: Regularly provide learning reports
Applicable scenario: A small number of students begin their study

Plan B: Regularly provide reports + teaching exchange
Applicable scenario: Intention to initiate 'teaching collaboration'
Advantages: OSOC provides targeted solutions for teaching collaboration

Plan C: Regularly provide reports + teaching exchange + assign TAs
Applicable scenario: A certain number of students are studying, and they form study groups
Advantages: Assign TAs to monitor student progress within the group and provide guidance and support

Plan D: Achieve OSOC credit certification
Applicable scenario: University officially recognize OSOC learning contents and award credits on it
Advantages: Combines students' extracurricular practice with academic credits, effectively motivating students to participate in

Plan E: Set OSOC club/workshop
Advantages: Officially make study study group and OSOC could provide some financial support

Plan F: Integrate OSOC tools in courses
Applicable scenario: University adjusts courses to integrate relevant contents

Plan G: Integrate OSOC experiments in courses
Advantages: Enhance practical aspects of the class, develop students' hands-on skills

Plan H: Offer OSOC Practical Courses
Advantages: Comprehensively cultivate students' knowledge across the entire front-end and back-end chain, as well as their hands-on practical skills

Plan I: Offer OSOC Bootcamp
Applicable scenario: University provides venue and resource support, while OSOC provides teaching organization
Advantages: Concentrated offline teaching and learning for students, with high learning efficiency, short duration

Plan J: Conduct research and teaching project collaboration
Applicable scenario: University and OSOC share common project collaboration goals
Advantages: Both parties contribute resources to tackle technical challenges and carry out research and development, with project validation and iteration experience used for curriculum reform

The plans are gradually deepened and can also be carried out at the same time.

Future Plan

- Invite or **attract more domestic and overseas students** to participate
- **Improve and add more language versions of handouts**
 - including but not limited to: Portuguese, Japanese, German, Russian, etc.
- **Establish deeper cooperation with some universities (domestic and overseas)**
 - form large-scale study groups and workshops
 - introduce OSOC experiments in courses or as part of graduation projects
- **Connect more companies and institutions**
 - provide greater and better employment opportunities for advanced-level students
- **Set overseas bases**
 - provide venue for local students to gather and study offline



Thank you!

For collaboration and communication,
please contact via email:

suxiaoke@ict.ac.cn



website
[**ysyx.org/en**](http://ysyx.org/en)



Telegram
Group Chat



中国科学院大学
University of Chinese Academy of Sciences



中国科学院计算技术研究所
INSTITUTE OF COMPUTING TECHNOLOGY, CHINESE ACADEMY OF SCIENCES



北京开源芯片研究院
BEIJING INSTITUTE OF OPEN SOURCE CHIP

FAQ



More FAQs

- Q: Where can I register?

A: On the official website(ysyx.org/en), follow the signup process.

- Q: Where can I find the study materials?

A: On the official website(ysyx.org/docs/en/)

- Q: I am in a lower grade/attending an ordinary university/studying another major/have no prior knowledge, can I participate?

A: Yes, you can.

- Q: I have already graduated, can I participate?

A: You could study as you want, but free tape-out will be only provided for students.

- Q: When is the registration deadline?

A: It's open all the time, you can learn anytime.

- Q: Are there any fees for registration and learning?

A: This is a free project — no fees will be charged.

- Q: How is registration screened?

A: There is no screening, the project team encourages everyone to learn.

- Q: How long does it usually take to study?

A: It varies from person to person, you can try for two weeks first.

- Q: When do I need to finish the learning?

A: There is no deadline, finish the learning and apply for defense.